Power Quotient International

IC STORAGE SPECIALIST

Datasheet for DOM

TDK DiskOnModule 019 Series

PQI Product No:

FDXXX-019P(R).XD4

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Power Quotient International Co., Ltd.

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Power Quotient International
— IC STORAGE SPECIALIST

DiskOnModule™ Series
Preliminary

4MB/8MB/16MB/32MB/48MB
64MB/96MB/128MB/192MB/256MB

DESCRIPTION

FDXXX-XXX.XD4 series is PQI's ***DiskOnModule*** based on TDK NAND Type flash memory controller technology. This product complies with 40/44 PIN IDE (ATA) standard interface and is suitable for data storage memory medium for portable system. By using ***DiskOnModule*** it is possible to operate good performance for the portable system which have IDE interface slots.

FEATURES

- High Performance
- Non-volatile Flash Memory
  The DOM is implemented by using NAND type flash memory, which is a high density, non-volatile read/write device. Flash data retention is guaranteed for at least 10 years, with no battery or other power source required.
- 100% True Mode IDE HDD Compatible
- Broad Operating System and Processors Supports
- Capacities 4~256Mbytes
- Low Power Consumption
- Robust Error Correction
- High Reliability

*Design with TDK GBDriver series product to access NAND type flash memory.

INTRODUCTION

1.About This Manual

This manual provides instructions for the installation and specification of PQI's ***DiskOnModule, DiskOnModule*** is designed for use in PCs, and their respective compatible computers.

2.What is *DiskOnModule*?

PQI's ***DiskOnModule*** is a storage device based on flash memory technology, which emulates an ordinary magnetic hard disk. The ***DiskOnModule*** series products provide an all in one module solution for solid-state flash disk. The ***DiskOnModule*** is suitable for use in portable and embedded systems which have limited space and power consumption.

Unlike standard IDE drives, no signal cable and extra, special space is required. The ***DiskOnModule*** is a solid-state solution for IDE Hard Disk drive, which has no moving parts. That provides a good stability in a moving system. The ***DiskOnModule*** products are also free from extra and special algorithm or some firmware driver. Just plug the ***DiskOnModule*** into the IDE slot and play it, users can play the ***DiskOnModule*** as same as the Hard Disk Drives.

The ***DiskOnModule*** family provides the capacities ranging from 4MB up to 256MB. In the future, the capacity will be increased up to 512MB.

SPECIFICATION

Environment Specifications

Temperature	Operating	0℃ to +70℃
	Non-Operating	-20℃ to +85℃
Relative Humidity		8% to 95% (with no condensation)
Vibration	Operating	15G
	Non-operating	15G
Shock	Operating	50G
	Non-operating	1000G

Configuration

Capacity	4Mbytes to 256Mbytes
Sector size	512Bytes

System Performance

Media transfer rate	write	1.2MB/sec (typ.)
	read	4.1 MB/sec (typ.)
Interface burst transfer rate		
PIO mode 2		8.3 MB/sec (max)

Reliability

MTBF(@25℃)	300,000 hours
ECC	22bit per 256bytes

Power Requirement

Voltage	DC +3.3V±5%(Option)
	DC +5.0V±10%

Power Consumption

Read	21mA (typ.)
Write	28mA (typ.)
Sleep	0.3mA (typ.)

Physical specifications

Reference P

Capacity Specifications

Capacity	No. of Cylinders	No. of Sectors/Track	No. of Heads	Unformated Capacity (Bytes)
4MB	250	16	2	4096000
8MB	500	16	2	8192000
16MB	1000	16	2	16384000
24MB	750	16	4	24576000
32MB	500	16	8	32768000
48MB	750	16	8	49152000
64MB	500	32	8	65536000
96MB	750	32	8	98304000
128MB	500	32	16	131072000
192MB	380	63	16	196116480
256MB	507	63	16	261660672

INSTALLTION GUIDE

BEFORE YOU BEGIN

To protect your DOM from static discharge by making sure you are well grounded before touching the DOM. We recommend wearing a grounded wrist strap throughout the installation process.

STEP 1

1. Make sure your computer is turned off before you open the case.
2. Plug the DOM carefully into the IDE slot on your computer or host adapter.
   Caution: Make sure to align pin1 on the computer or host adapter interface connector with pin 1 on your DOM. Pin 1 is indicated by a triangle on the DOM connector.
3. Connect the power cable of the DOM to an unused power connector of the computer.
   Caution: If you need to remove your DOM, use **BOTH HANDS** to carefully pull out it.
4. Check all cable connections and then replace your computer cover.

STEP 2

Before you format or partition your new drive, you must configure your computer's BIOS so that the computer can recognize your new drive.

1. Turn your computer on. As your computer start up, watch the screen for a message describing how to run the system setup program (sometimes called BIOS or CMOS setup). This is usually done by pressing a special key, such as DELETE,ESC, or F1, during startup. See your computer manual for details. Press the appropriate key to run the system setup program.
2. If your BIOS provides automatic drive detection (an "AUTO" drive type), select this option. (We recommend that use Normal/CHS mode to partition your DOM to get the maximum formatted capacity.)
   This allows your computer to configure itself automatically for your new drive.
   If your BIOS dose not provide automatic drive detection, select "User-defined" drive setting and enter the CHS values from the table.
   BIOS Settings (see specification)
   Capacity Cylinders Heads Sectors
   (unformatted)
3. Save the settings and exit the System Setup program.
   (your computer will automatically reboot)
   After you configure your computer, you can use the standard DOS commands to partition and format your DOM, as described below.

STEP 3

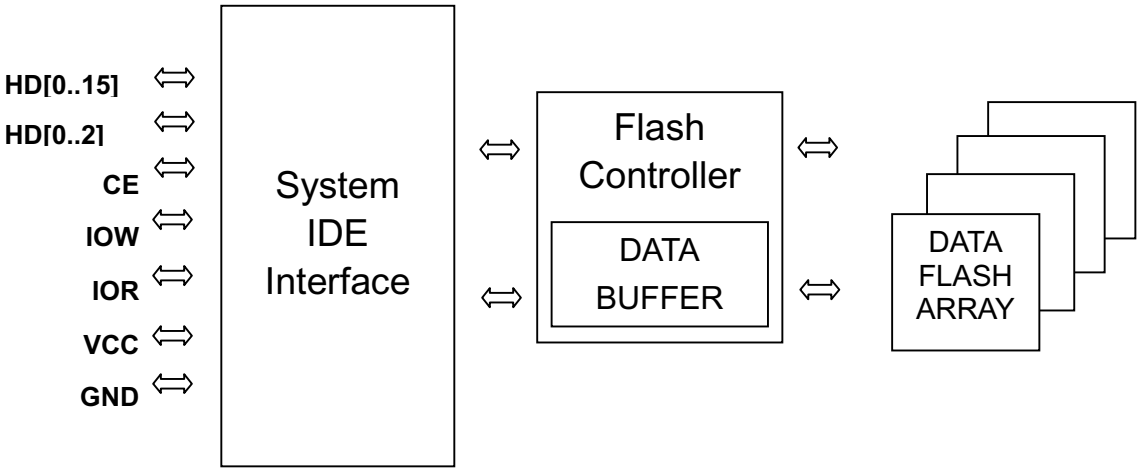
To partition your new DOM with Microsoft® DOS program :

1. Insert a bootable DOS diskette into your diskette drive and restart your computer.
2. Insert a DOS program diskette that contains the **FDISK.EXE** and **FORMAT.COM** programs into your diskette drive. Use the same DOS version that is on your bootable diskette. At the A: prompt, type **FDISK** and press **ENTER**.
3. If you have two **IDE** devices installed, the **FDISK** menu displays five options. Option five allows you to select the drive you want to partition. Make sure that your new drive is selected.
4. Select "Create DOS partition or logical DOS drive" by pressing 1. Then press ENTER.
5. Select "**Create primary DOS partition**" by pressing **1** again. Then press **ENTER**. Create your first drive partition. If you are creating a partition that will be used to boot your computer (drive C), make sure that the partition is marked active.
6. Create an extended partition and additional logical drives as necessary, until all the

space on your new hard drive has been partitioned.

7. When the partitioning is complete, **FDISK** reboots your computer.
   Caution: Make sure to use the correct drive letters so that you do not format a drive that already contains data.
8. At the A: prompt, type **format c:/s**, where c is the letter of your first new partition, Repeat the format process for all the new partitions you have created.
9. After you format your drive, it is ready to use.

Block Diagram



The external ROM can be eliminated to be one chip solution by way of next generation of flash controller.

About Our Flash Management

In order to gain the best management for flash memory, PQI ***DiskOnModule*** supports an efficient and swift algorithm. Due to the life of flash memory is limited, PQI try to increase the life of our flash product through the following arrangement. There are some blocks are reserved in flash memory and these blocks would not be used in normal operation. Once any block is fail, one of these reserved blocks will replace it and the data of the fail block would be transferred to the reserved block for keeping the data's accuracy. After we used the above arrangement in flash memory, the life of the device will be longer than the device without it. When all of the reserved blocks have replaced the bad blocks, the device will be locked automatically to prevent programming, but the data can still be read out for back up.

Because the block of flash memory has a limited life, when the host writes data in the same address, PQI ***DiskOnModule*** does not to program data into the same physical place of the flash memory in purpose, our algorithm will get the data precisely when the host wants to read the data.

ECC (Error Correction Code) feature also be built in our hardware and firmware, it will correct 1 bit errors, and detect 2 bits errors when they happened. ECC ensured the accuracy of the data, and decreased the effect of the cross talking on the bus.

Based on the latest hardware and firmware, PQI DiskOnModule device can be up to 1.2MB/sec in writing data into medium, and be up to 4.1MB/sec in reading data from medium.

44/40 Pin Signal Assignment

The signals assigned for 44/40-pin applications are described in Table 1

Table 1 – Signal assignments for 44-pin ATA

Signal name	Connector contact	Conductor		Connector contact	Signal name
RESET-	1	1	2	2	Ground
DD7	3	3	4	4	DD8
DD6	5	5	6	6	DD9
DD5	7	7	8	8	DD10
DD4	9	9	10	10	DD11
DD3	11	11	12	12	DD12
DD2	13	13	14	14	DD13
DD1	15	15	16	16	DD14
DD0	17	17	18	18	DD15
Ground	19	19	20	20	(keypin)
DMARQ	21	21	22	22	Ground
DIOW-	23	23	24	24	Ground
DIOR-	25	25	26	26	Ground
IORDY	27	27	28	28	CSEL
DMACK-	29	29	30	30	Ground
INTRQ	31	31	32	32	reserved
DA1	33	33	34	34	PDIAG-
DA0	35	35	36	36	DA2
CS0-	37	37	38	38	CS1-
DASP-	39	39	40	40	Ground
+5 V (logic) (see note)	41	41	42	42	+5 V (Motor) (see note)
Ground(return) (see note)	43	43	44	44	TYPE- (0=ATA) (see note)
NOTE – Pins which are additional to those of the 40-pin cable.					

Interface Signal Assignments And Descriptions

Signal summary

The physical interface consists of receivers and drivers communicating through a set of conductors using an asynchronous interface protocol. Table 2 defines the signal names.

Table 2 - Interface signal name assignments

Description	Host	Dir	Dev	Acronym
Cable select	(see note)			CSEL
Chip select0	→			CS0-
Chip select1	→			CS1-
Data bus bit 0	↔			DD0
Data bus bit 1	↔			DD1
Data bus bit 2	↔			DD2
Data bus bit 3	↔			DD3
Data bus bit 4	↔			DD4
Data bus bit 5	↔			DD5
Data bus bit 6	↔			DD6
Data bus bit 7	↔			DD7
Data bus bit 8	↔			DD8
Data bus bit 9	↔			DD9
Data bus bit 10	↔			DD10
Data bus bit 11	↔			DD11
Data bus bit 12	↔			DD12
Data bus bit 13	↔			DD13
Data bus bit 14	↔			DD14
Data bus bit 15	↔			DD15
Device active or slave (Device 1) present	(see note)			DASP-
Device address bit 0	→			DA0
Device address bit 1	→			DA1
Device address bit 2	→			DA2
DMA acknowledge	→			DMACK-
DMA request	←			DMARQ
Interrupt request	←			INTRQ
I/O read	→			DIOR-

I/O ready	←	IORDY
I/O write	→	DIOW-
Passed diagnostics	(see note)	PDIAG-
Reset	→	RESET-
NOTE – See signal descriptions for information on source of these signals		

Signal Descriptions

CS0- (CHIP SELECT 0)

This is the chip select signal from the host used to select the Command Block registers.

CS1 – (CHIP SELECT 1)

This is the chip select signal from the host used to select the Control Block registers.

DA2, DA1, AND DA0 (DEVICE ADDRESS)

This is the 3-bit binary coded address asserted by the host to access a register or data port in the device.

DASP – (Device active, device 1 present)

This is a time-multiplexed signal which indicates that a device is active, or that Device 1 is present. This signal shall be an open collector output and each device shall have a 10 kΩ pull-up resistor.

If the host connects to the DASP- signal for the illumination of an LED or for any other purpose, the host shall ensure that the signal level seen on the ATA interface for DASP- shall maintain V_{OH} and V_{OL} compatibility, given the I_{OH} and I_{OL} requirements of the DASP- device drivers.

DD (15:0) (Device data)

This is an 8- or 16-bit bi-directional data interface between the host and the device. The lower 8 bits are used for 8-bit register transfers.

DIOR- (Device I/O read)

This is the read strobe signal from the host. The falling edge of DIOR- enables data from the device onto the signals, DD (7:0) or DD (15:0). The rising edge of DIOR- latches data at the host and the host shall not act on the data until it is latched.

DIOW- (Device I/O write)

This is the Write strobe signal from the host. This rising edge of DIOW- latches data from the signals, DD (7:0) or DD (15:0), into the device. The device shall not act on the data until it is latched.

DMACK- (DMA acknowledge)

This signal shall be used by the host in response to DMARQ to initiate DMA transfers.

DMARQ (DMA request)

This signal, used for DMA data transfer between host and device, shall be asserted by the device when it is ready to transfer data to or from the host. The direction of data transfer is controlled by DIOR- and DIOW-. This signal is used in a handshake manner with DMACK- i.e., the device shall wait until the host asserts DMACK- before negating DMARQ, and re-asserting DMARQ if there is more data to transfer.

This line shall be released (high impedance state) whenever the device is not selected or is selected and no DMA command is in progress. When enabled by DMA transfer, it shall be driven high and low by the device.

When a DMA operation is enabled, CS0- and CS1- shall not be asserted and transfers shall be 16-bits wide.

INTRQ (Device interrupt)

This signal is used to interrupt the host system. INTRQ is asserted only when the device has a pending interrupt, the device is selected, and the host has cleared the nIEN bit in the Device Control register. If the nIEN bit is equal to one, or the device is not selected, this output is in a high impedance state, regardless of the presence or absence of pending interrupt.

The pending interrupt condition shall be set by:

- the completion of a command; or
- at the beginning of each data block to be transferred for PIO transfers except for the first data block for FORMAT TRACK. WRITE SECTOR(S), WRITE BUFFER, and WRITE LONG commands.

The pending interrupt condition shall be cleared by:

- assertion of RESET-; or
- the setting of the SRST bit of the Device Control register; or
- the host writing the Command register; or
- The host reading the Status register.

IOCS 16- (Device 16-bit I/O)

Obsolete.

IORDY (I/O channel ready)

This signal is negated to extend the host transfer cycle of any host register access (Read or Write) when the device is not ready to respond to a data transfer request.

If actively asserted, the signal only be enabled during DIOR-/DIOW- cycles to the selected device. If open collector, when IORDY is not negated, it shall be in the high-impedance (undriven) state.

This use of IORDY is required for PIO modes 3 and above and otherwise optional.

PDIAG - (Passed diagnostics)

This signal shall be asserted by Device 1 to indicate to Device 0 that it has completed diagnostics. A 10 kΩ pull-up resistor shall be used on this signal by each device.

The host shall not connect to the PDIAG-signal.

RESET- (Device reset)

This signal from the host system shall be asserted beginning with the application of power and held asserted until at least 25 μs after voltage levels have stabilized within tolerance during power on
and negated thereafter unless some event requires that the device(s) be reset following power on.

ATA devices shall not recognize a signal assertion shorter than 20 ns valid reset signal. Devices may respond to any signal assertion greater than 20 ns, and shall recognize a signal equal to or greater than 25 μs.

CSEL (Cable select)

The device is configured as either Device 0 or Device 1 depending upon the value of CSEL.

Interface Register Definitions And Descriptions

Device addressing considerations

In traditional controller operation, only the selected device receives commands from the host following selection. In this standard, the register contents go to both devices (and their embedded controllers.) The host discriminates between the two by using the DEV bit in the Device/Head register.

Data is transferred in parallel either to or from host memory to the device's buffer under the direction of commands previously transferred from the host. The device performs all of the operations necessary to properly write data to, or read data from, the media. Data read from the media is stored in the device's buffer pending transfer to the host memory and data is transferred from the host memory to the device's buffer to be written to the media.

The devices using this interface shall be programmed by the host computer to perform commands and return status to the host at command completion. When two devices are daisychained on the interface, commands are written in parallel to both devices, and for all except the EXECUTE DEVICE DIAGNOSTICS command, only the selected device executes the command. On an EXECUTE DEVICE DIAGNOSTICS command addressed to Device 0, both devices shall execute the command, and Device 1 shall post its status to Device 0 via PDIAG-.

Devices are selected by the DEV bit in the Device/Head register. When the DEV bit is equal to zero, Device 0 is selected. When the DEV bit is equal to one, Device 1 is selected. When devices are daisy chained, one shall be set as Device 0 and the other as Device 1.

I/O register descriptions

Communication to or from the device is through an I/O Register that routes the input or output data to or from registers addressed by the signals from the host (CS0-, CS1-, DA (2:0), DIOR-, AND DIOW-).

The Command Block Registers are used for sending commands to the device or posting status from the device. The Control Block Registers are used for device control and to post alternate status.

Anytime a command is in progress, that is, from the time the Command register is written until the device has completed the command and posted ending status, the device shall have either BSY or DRQ set to one. If the Command Block registers are read by the host when BSY or DRQ is set to one, the content of all register bits and fields except BSY and DRQ in the Status and Alternate Status registers is indeterminate. If the host writes to any Command Block register when BSY or DRQ is set to one, the results are indeterminate and may result in the command in progress ending with a command abort error.

When performing PIO transfers, BSY and DRQ shall both be cleared to zero within 400 ns of the transfer of the final byte of data. This assertion signals the completion of a PIO data transfer command.

Table 3 lists these registers and the addresses that select them.

Table 3 - I/O port functions and selection address

Addresses					Functions	
CS0-	CS1-	DA2	DA1	DA0	Read (DIOR-)	Write (DIOW-)
N	N	×	×	×	Data bus high impedance	Note used
					Control block registers	
N	A	0	×	×	Data bus high impedance	Note used
N	A	1	0	×	Data bus high impedance	Note used
N	A	1	1	0	Alternate Status	Device Control
N	A	1	1	1	(see note1)	Not used
					Command block registers	
A	N	0	0	0	Data	Data
A	N	0	0	1	Error	Features
A	N	0	1	0	Sector Count	Sector Count
A	N	0	1	1	Sector Number LBA (7:0) (see note 2)	Sector Number LBA (7:0) (see note 2)
A	N	1	0	0	Cylinder Low LBA (15:8) (see note 2)	Cylinder Low LBA (15:8) (see note 2)
A	N	1	0	1	Cylinder High LBA (23:16) (see note 2)	Cylinder High LBA (23:16) (see note 2)
A	N	1	1	0	Device/Head LBA (27:24) (see note 2)	Device/Head LBA (27:24) (see note 2)
A	N	1	1	1	Status	Command
A	A	×	×	×	Invalid address	Invalid address

Key:
A = signal asserted, N = signal negated, × = don't care
NOTES_
1 This register is obsolete. It is recommended that a device not respond to a read of this address. If a device does respond, it shall not drive the DD7 signal to prevent possible conflict with floppy disk implementations.
2 Mapping of registers in LBA translation.

Each register description in the following clauses contain the following format:

ADDRESS – the CS and DA address of the register.

DIRECTION – indicates if the register is read/write, read only, or write only from the host.

ACCESS RESTRICTIONS – indicates when the register may be accessed.

EFFECT – indicates the effect of accessing the register.

FUNCTIONAL DESCRIPTION – describes the function of the register.

FIELD/BIT DESCRIPTION – describes the content of the register.

[Duplicate Data, Error and Feature register]

During word access, the address space occupied by the Data Register interferes with the space occupied by the Error register and Feature register, and reference cannot be made to these registers. Therefore, the PC Card ATA Standard provides an area where the copy of each register does not duplicate in the contiguous I/O mode and memory map mode. The even-numbered address of the data register is provided in the offset "08h", and the odd-numbered address of the data register is located in the offset "09h". The copy of Error/Feature register is provided at the ODh.

Duplicate Data register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data Word															
Odd Data Byte Only								Even or Even-Odd Data Byte							

Duplicate registers Access

Data register	CE2#	CE#	A0	Offset	Data Bus
Word Data register	0	0	0	0h,8h	D15-D0
Word Data register	0	0	1	1h,9h	D15-D0
Even Byte Data register	1	0	0	0h,8h	D7-D0
Odd Byte Data register	1	0	1	9h	D7-D0
Odd Byte Data register	0	1	×	8h,9h	D15-D8
Error/Feature register	1	0	1	1h,0Dh	D7-D0
Error/Feature register	0	1	×	0h,1h	D15-D8
Error/Feature register	0	0	×	0Ch,0Dh	D15-D8

Initial value of task file register

After resetting and execution of the Execute Device Diagnostic command, the task file register is initialized as follows:

Sector Count register 01h
Sector Number register 01h
Cylinder Lo register 00h
Cylinder High register 00h
Device/Head register A0h

PIO Data Transfers

Figure 1 defines the relationships between the interface signals for PIO data transfers. Peripherals reporting support for PIO Transfer Mode 3 or 4 shall power up in a PIO Transfer Mode 0, 1, or 2.

For PIO modes 3 and above, the minimum value of t0 is specified by word 68 in the IDENTIFY DEVICE parameter list.

IORDY shall be supported when PIO Mode 3 or 4 are the current mode of operation.

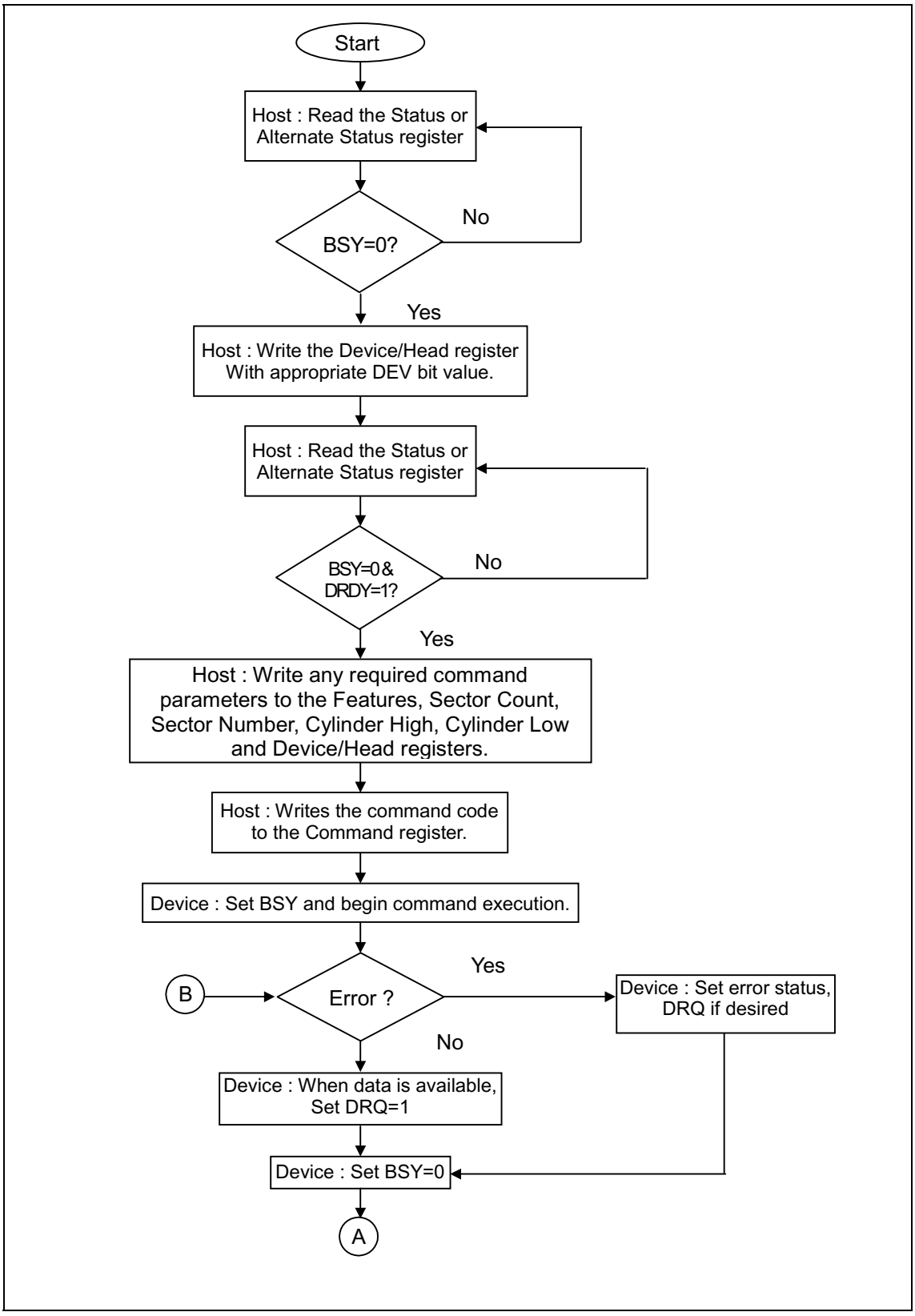


Figure 2 – PIO data transfer in diagram

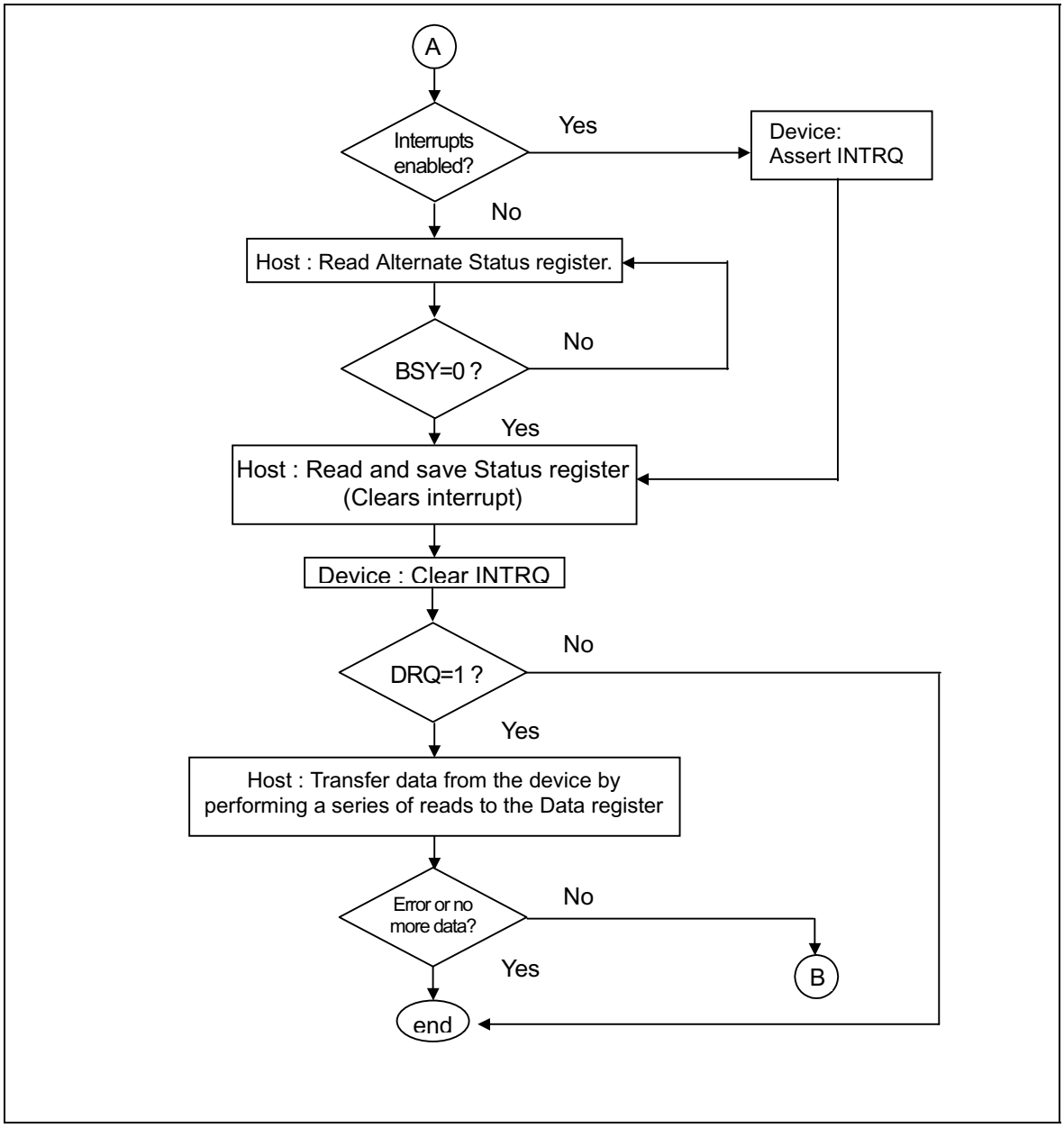


Figure 3 – PIO data transfer in diagram (concluded)

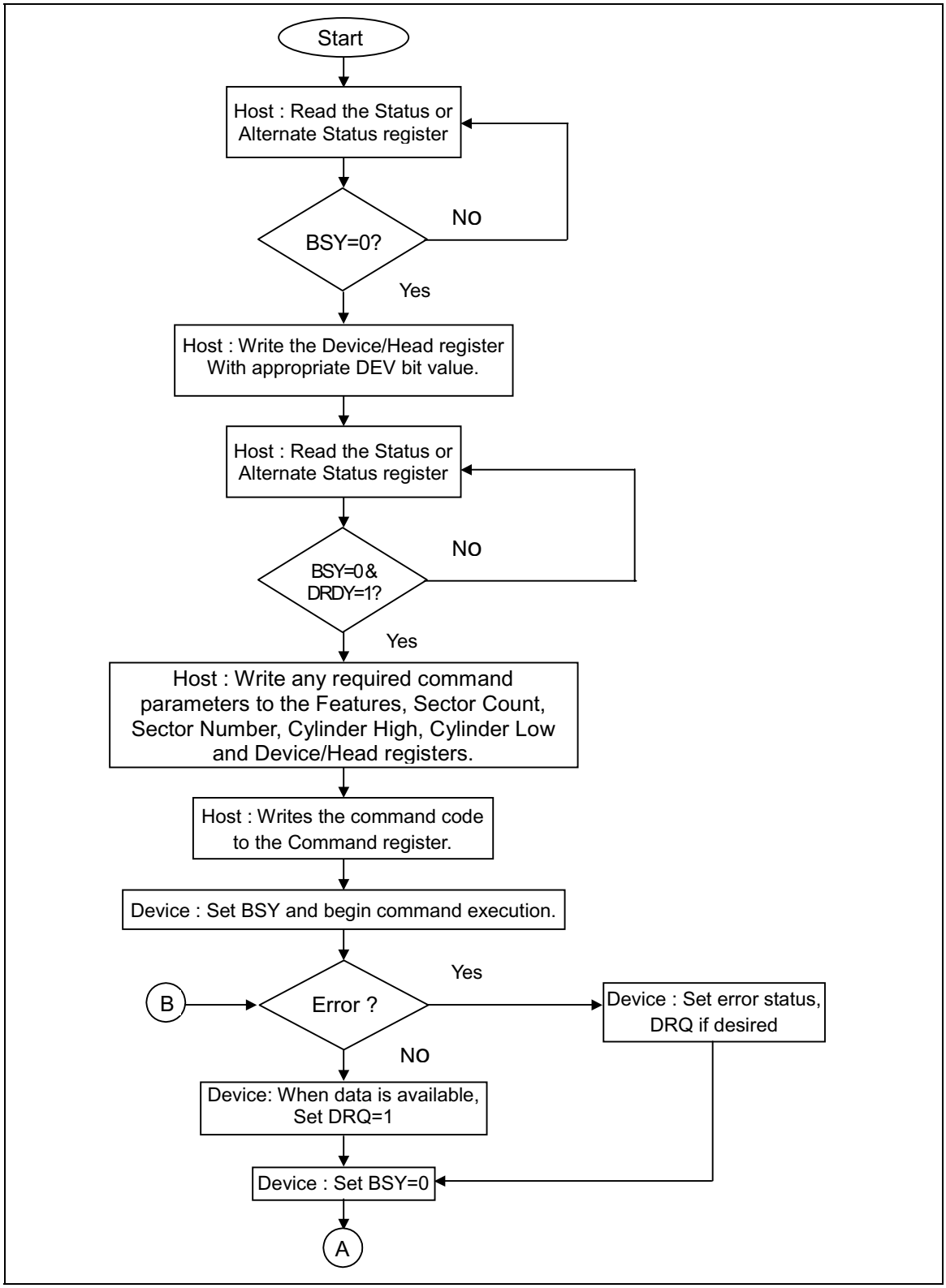


Figure 4 – PIO data transfer out diagram (continued)

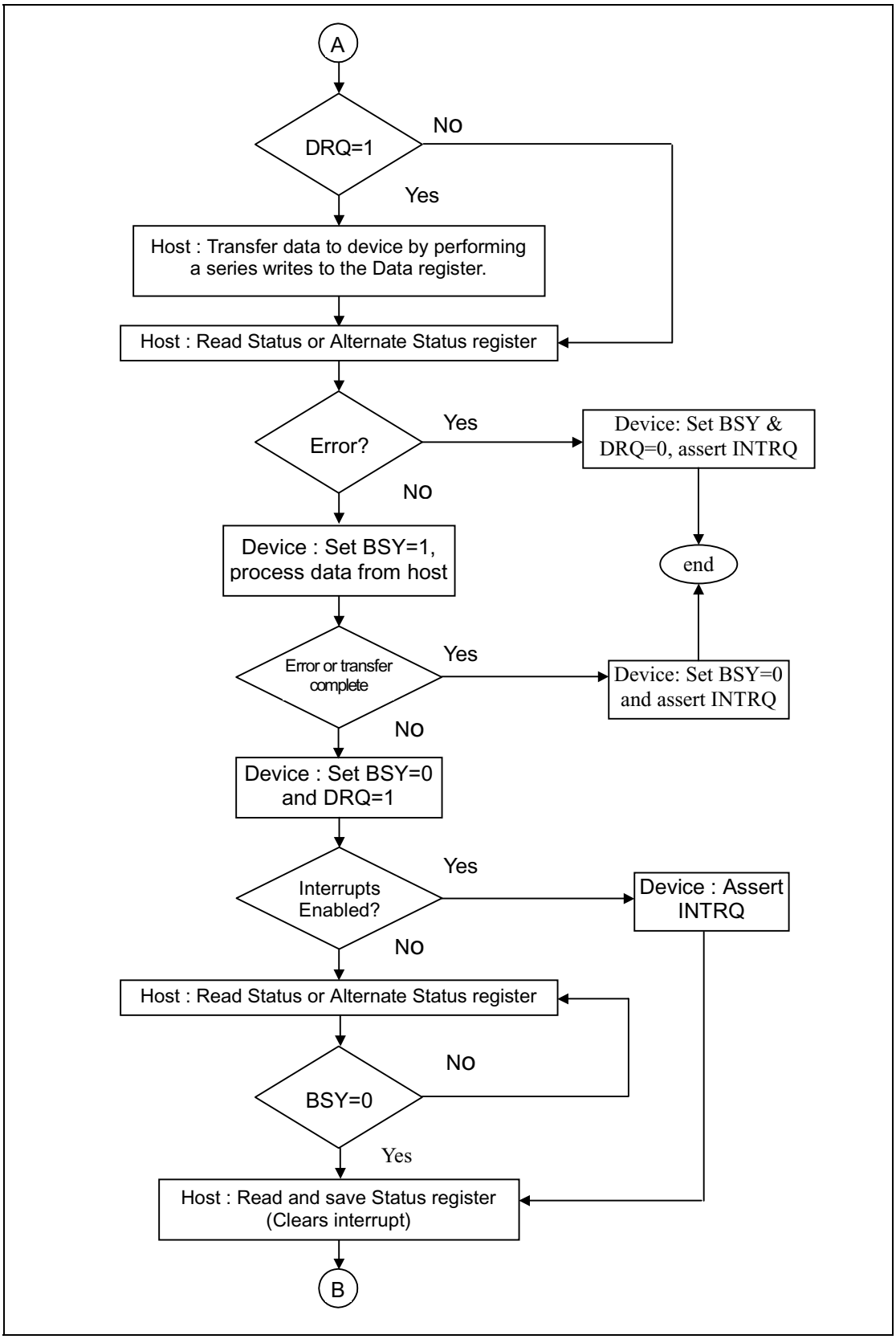
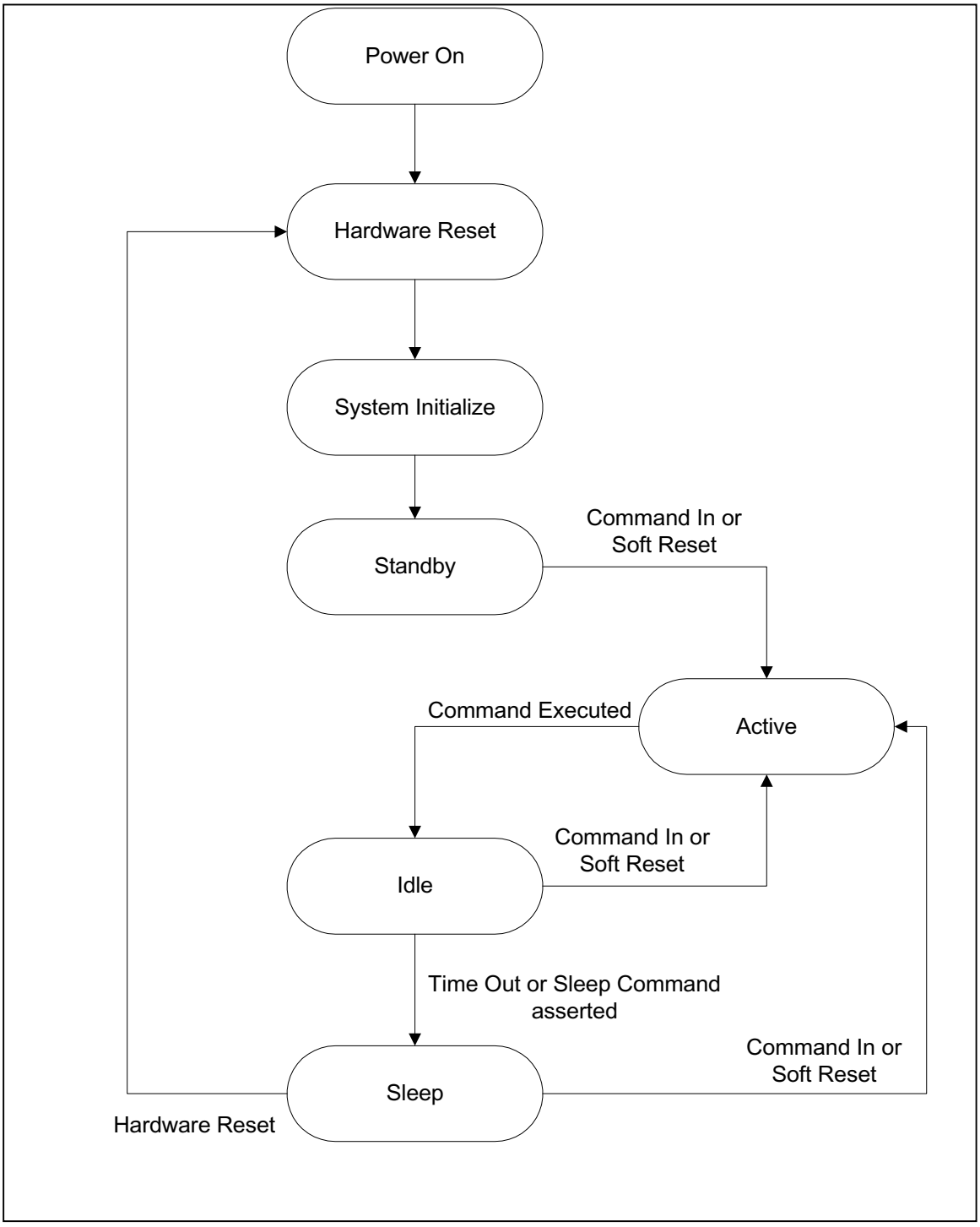


Figure 5 – PIO data transfer out diagram (concluded)

Power Saving Flow:



G. Electrical Specifications

Absolute Maximum Rating

Item	Symbol	Parameter	MIN	MAX	Unit
1	V_{DD}-V_{SS}	DC Power Supply	-0.3	+5.5	V
2	V_{IN}	Input Voltage	V_{SS}-0.3	V_{DD}+0.3	V
3	Ta	Operating Temperature	0	+70	℃
4	Tst	Storage Temperature	-55	+150	℃

H. DC Specifications

H.1. DC Characteristics-1 (Ta=0 to +70℃, V_{CC}= 3.3V ± 10%)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Input Voltage	VIH	--	0.7×V_{CC}	--	V_{CC} +0.3	V
	VIL	--	-0.3	--	0.2×V_{CC}	V
Output Voltage IOL = 3mA (*1)	VOH	IOL = -3mA	V_{CC} –0.4	--	--	V
	VOL	IOL = 3mA	--	--	0.4	V
Input leakage current (*2)	ILK	VIH = VDD / VIL = GND	-1	--	1	uA
Sleep current(*3)	ISP	Control signal = V_{CC} – 0.2	--	180	--	uA
Sector read current (*4,*3)	ISR(DC)	Control signal = V_{CC} – 0.2	--	20	--	mA
	ISR(Peak)		--	40	--	mA
Sector write current (*5,*3)	ISW(DC)	Control signal = V_{CC} – 0.2	--	25	--	mA
	ISW(Peak)		--	50	--	mA

H.2. DC Characteristics-1 (Ta=0 to +70℃, V_{CC}= 5.0V ± 10%)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Input Voltage	VIH	--	0.7×V_{CC}	--	V_{CC} +0.3	V
	VIL	--	-0.3	--	0.3×V_{CC}	V
Output Voltage IOL = 3mA (*1)	VOH	IOL = -3mA	V_{CC} –0.4	--	--	V
	VOL	IOL = 3mA	--	--	0.4	V
Input leakage current (*2)	ILK	VIH = VDD / VIL = GND	-1	--	1	uA
Sleep current(*3)	ISP	Control signal = V_{CC} – 0.2	--	450	--	uA
Sector read current (*4,*3)	ISR(DC)	Control signal = V_{CC} – 0.2	--	40	--	mA
	ISR(Peak)		--	80	--	mA
Sector write current (*5,*3)	ISW(DC)	Control signal = V_{CC} – 0.2	--	55	--	mA
	ISW(Peak)		--	110	--	mA

Note : 1.Measured for static state.

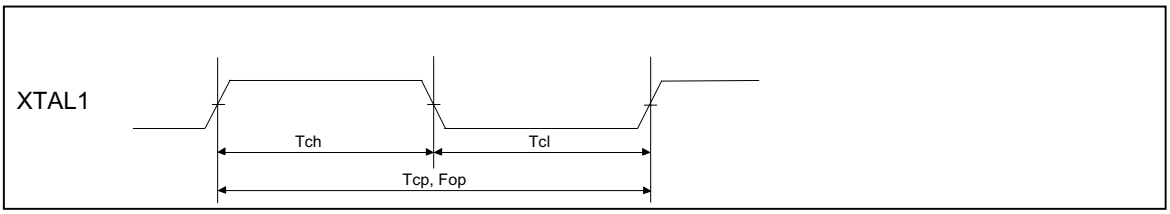
2.Except pulled up input/output pin.

3.Power dissipation is reference value on the assembled flash card, including the flash memory.

4.Measured during sector read transfer.

5.Measured during sector write transfer.

Clock Input Timing



Symbol	Parameter	Min	Max	Unit
Fop	Operating Speed	0	25	MHz
Tcp	Clock Period	40	-	ns
Tch	Clock High	18	-	ns
Tcl	Clock Low	18	-	ns

ATA command

Commands to be supported

This card shows the ATA command and CF ATA command supported by this card:

Supported ATA Commands List

Class	Command		Code	Registers					
				FR	SC	SN	CY	DH	LBA
1	Check Power Mode		98h,E5h	-	-	-	-	D	-
1	Execute Drive Diagnostic	Essential	90h	-	-	-	-	-	-
2	Format Track (CHS/LBA)	Essential	50h	-	(-/Y)	(-/Y)	Y	Y	Y
1	Identify Drive		ECh	-	-	-	-	D	-
1	Idle		97h,E3h	-	Y	-	-	D	-
1	Idle Immediate		95h,E1h	-	-	-	-	D	-
1	Initialize Drive Parameters	Essential	91h	-	Y	-	-	Y	-
1	Recalibrate	Essential	1Xh	-	-	-	-	D	Y
1	Read Buffer		E4h	-	-	-	-	D	-
1	Read Multiple		C4h	-	Y	Y	Y	Y	Y
1	Read Sector(s)	Essential	20h,21h	-	Y	Y	Y	Y	Y
1	Read Long	Essential	22h,23h	-	Y	Y	Y	Y	Y
1	Read Verify Sector(s)	Essential	40h,41h	-	Y	Y	Y	Y	Y
1	Seek	Essential	7Xh	-	-	Y	Y	Y	Y
1	Set Features		EFh	Y	-	-	-	D	-
1	Set Multiple Mode		C6h	-	Y	-	-	D	-
1	Set Sleep Mode		99h,E6h	-	-	-	-	D	-
1	Standby (CF/SmartMedia)		96h,E2h	-	(-/Y)	-	-	D	-
1	Standby Immediate		94h,E0h	-	-	-	-	D	-
2	Write Buffer		E8h	-	-	-	-	D	-
3	Write Multiple		C5h	-	Y	Y	Y	Y	Y
2	Write Sector(s)	Essential	30h,31h	-	Y	Y	Y	Y	Y
2	Write Long	Essential	32h,33h	-	Y	Y	Y	Y	Y
3	Write Multiple Without Erase		CDh	-	Y	Y	Y	Y	Y
1	Request Sense		03h	-	-	-	-	D	-
1	Translate Sector		87h	-	-	Y	Y	Y	Y
1	Security Disable Password	CF only	F6h	-	-	-	-	D	-
1	Security Erase Password	CF only	F3h	-	-	-	-	D	-
1	Security Erase Unit	CF only	F4h	-	-	-	-	D	-
1	Security Freeze Lock	CF only	F5h	-	-	-	-	D	-
1	Security Set Password	CF only	F1h	-	-	-	-	D	-
1	Security Unlock	CF only	F2h	-	-	-	-	D	-
1	Wear Level		F5h	-	-	-	-	D	-
3	Write Verify		3Ch	-	Y	Y	Y	Y	Y
1	Erase Sector(s)		C0h	-	Y	Y	Y	Y	Y
2	Write Sector(s) Without Erase		38h	-	Y	Y	Y	Y	Y

FR: Feature Register SC: Sector Count register SN: Sector Number register CY: Cylinder Registers DH: Device/Head register

Y: The value effective to execute commands is set to the register. The "Y" of the Device/Head register indicates that the parameters of both the Drive and Head are used.
D: Only the device parameters are valid. Head parameters are ignored.
-: Reference is not made to this register.

• **Occurrence of multiple command inputs**

When a new command is issued to this device during execution of the prior command, the command not yet completed is interrupted to accept the new command.
As writing into the command register is ignored during the BSY output period, this situation does not take place in the commands other than the media access related command. During execution of the media access related command, this device interrupts the preceding command immediately when another command is written in the BSY release period. If the command is interrupted just during being written into the flash memory, that block is erased and the old block before writing is recovered. If the interrupt is occurred during erasing flash memory, controller waits until erasure is completed. This device has a feature to keep consistency in the flash memory management system even in case of interrupted command. Controller has function to recover the old status so long as erasure of the old user area is not started. But to ensure reliability, when the command is issued, it is necessary to confirm by all means that the device is ready to accept the command (both DRQ and BSY released).

• **ATA command specifications**

(1) Check Power Mode (98h or E5h)

This is a command to return the current power mode. This device sets "00h" to the Sector Count register when in the sleep mode, and "FFh" to the Sector Count register when in the active mode. The power mode is not affected by the processing of this command.

Input parameter

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Command	98h or E5h							

Notation "na" indicates that reference is not made to the value by this command. (The same applies hereinafter).

Device/Head register: Specify drive number.

Output parameter at normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	result							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

The crosshatched section of the Status register and Error register indicates the bits which are not valid as a response to this command.

(The same applies hereinafter).

Status register : 50h

Sector Count register : 00h (Power is in the Standby or Sleep mode)

: FFh (Power is in the Idle mode)

Output parameter in abnormal completion

Register	7	6	5	4	3	2	1	0
Error	na					ABRT	na	
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

(Drive failure)

Status register : 11h

Error register : 04h(Aborted Command)

(2) Execute Drive Diagnostic (90h)

Upon receipt of this command, the controller resets all the connected flash memories in order to check the flash memory. The error state is indicated by the following Diagnostic codes. In the PC Card mode, the diagnostic result of this device alone is returned. The slave device is not supported. In the TrueIDE mode, the diagnostic result of this device is also returned only when this device is a master and the slave is present. For the way how the master gets the diagnostic results of the slave and how the diagnostic result is returned in the slave mode, see the ATA Standard. This command can be executed when the DRDY bit is not set.

Diagnostic Code after Power On Reset or Execute Drive Diagnostic command

Code	Description
01h	No error
02h	Format device error
03h	Sector buffer error
04h	ECC error
05h	Microprocessor control error
06h	Flash set error
07h	Fatal error in booting
8Xh	Slave error in TrueIDE

Input parameter

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na							
Command	90h							

The D4 (device number) of the Device/Head register is not evaluated.

This command is executed in both the master and slave modes.

Output parameter in normal and abnormal completion

Register	7	6	5	4	3	2	1	0
Error	Diagnostic code							
Sector Count	01h							
Sector Number	01h							
Cylinder Low	00h							
Cylinder High	00h							
Device/Head	00h							
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

The above result is output to the Error register.

There is no error report of this command itself.

Status register: 50h (10h when DRDY is not set)

(3) Format Track (50h)

This command is used to format the drive. In the LBA mode, this device provides format processing, using on the value set in the Sector Count register as a number of sectors for the specified track. In the CHS mode, the device provides format processing based on the number of sectors per track. This command is accompanied by the transfer of one sector alone. When the first bit of the transferred sector data is 00h, the write pattern 00h is written, and "FFh" is written at other times. The format pattern of each physical sector is determined by the first byte of the sector sent first. It should be noted, however, that use of this command is not recommended.

Input parameter

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	CHS:na/LBA:sector number to be formatted							
Sector Number	CHS:na/LBA:LBA[7:0]							
Cylinder Low	CHS:track number/LBA:LBA[15:8]							
Cylinder High	CHS:track number/LBA:LBA[23:16]							
Device/Head	na	LBA	na	DEV	CHS:Head/LBA[27:24]			
Command	50h							

CHS mode
Cylinder Low/High register : Track address to be formatted
Device/Head register : Track address, drive number and LBA flag to be formatted

LBA mode
Sector Count register : Number of sectors to be formatted (256 in the case of 00h)
Sector Number register : Sector address to be formatted LBA[7:0]
Cylinder Low register : Sector address to be formatted LBA[15:8]
Cylinder High register : Sector address to be formatted LBA[23:16]
Device/Head register : Sector address to be formatted LBA[27:24] drive number and LBA flag

Output parameter in normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	00h							
Sector Number	CHS:na/LBA:LBA[7:0]							
Cylinder Low	CHS:track number/LBA:LBA[15:8]							
Cylinder High	CHS:track number/LBA:LBA[23:16]							
Device/Head	na			DEV	CHS:Head/LBA[27:24]			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register : 50h
Sector Count register : 00h
Sector Number register : Last sector address LBA[7:0]
Cylinder Low register : Track address/last sector address LBA[15:8]
Cylinder High register : Track address/last sector address LBA[23:16]
Device/Head register : Track address/last sector address LBA[27:24]

Parameter name in abnormal completion

Register	7	6	5	4	3	2	1	0
Error	BBK	WP	MC	IDNF	MCR	ABRT	NM	AMNF
Sector Count	na							
Sector Number	CHS:na/LBA:LBA[7:0]							
Cylinder Low	CHS:track number/LBA:LBA[15:8]							
Cylinder High	CHS:track number/LBA:LBA[23:16]							
Device/Head	na			DEV	CHS:Head/LBA[27:24]			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

[Drive failure]
Status register : 11h
Error register : 04h(Aborted Command)

[Address overflow]
Status register : 51h
Error register : 10h(ID Not Found)
Sector Count register : Number of sectors unable to be formatted
Sector Number register : Address overflow LBA[7:0]
Cylinder Low register : Address overflow LBA[15:8]
Cylinder High : Address overflow LBA[23:16]
Device/Head register : Address overflow LBA[27:24]
Request Sense return value : 2Fh

[Timeout in write/erase operation]
Status register : 71h (31h, when an error has occurred in writing and an error has also occurred in immediately preceding writing and erasure)
Error register : 04h (Command abort)
Sector Count register : Number of sectors unable to be formatted
Sector Number register : Sector address where time has expired LBA[7:0]
Cylinder Low register : Sector address where time has expired LBA[15:8]
Cylinder High : Sector address where time has expired LBA[23:16]
Device/Head register : Sector address where time has expired LBA[27:24]
Request Sense return value : 03h

[Write/erase status error] (The erase status error occurs only in the case of FOh write failure into the redundancy part]
Status register : 71h (31h, when an error has occurred in writing and an error has also occurred in immediately preceding writing and erasure)
Error register : Number of sectors unable to be formatted
Sector Count register : Sector address where time has expired LBA[7:0]
Sector Number register : Sector address where time has expired LBA[15:8]
Cylinder Low register : Sector address where time has expired LBA[23:16]
Cylinder High register : Sector address where time has expired LBA[27:24]
Device/Head register : 03h
Request Sense return value

[Write protect error] (When the SmartMedia™ is set to the write protect status)
Status register : 71h
Error register : 40h (Write protected)
Request Sense return value : 03h

[Timeout error during table creation]
Status register : 11h
Error register : 04h (Aborted command)

[Physical block inspection error]
Status register : 71h
Error register : 04h(Aborted Command)
Request Sense return value : 0Ch

(4) Identify Drive (ECh)

This command is used for the host to get the drive parameter. For the drive parameter return value, see the separate Table. (The return value is different between the SmartMedia™ and CF modes).

Input parameter

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Command	ECh							

Device/Head register : Specify the drive number.

Output parameter in normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register : 50h

Output parameter in abnormal completion

Register	7	6	5	4	3	2	1	0
Error	na					ABRT	na	
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

[Drive failure]

Status register : 11h

Error register : 04h(Aborted Command)

(5) Idle (97h or E3h)

This command is used to place the device into the idle state according to ATA Standard. In this device, it is used only to change the setting of the automatic power down sequence. When the Sector Count register is not "00h", the automatic power down sequence is executed, and counting down is started immediately. (Shift to the automatic power down sequence is executed in the numerical value in the Sector Count register x about 5ms). When the Sector Count register is "00h", automatic power down sequence is disabled until the time of next resetting.

Input parameter

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Timer period value							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Command	97h or E3h							

Device/Head register : Specifies the drive number

Sector Count register : Constant value set on the automatic power reduction timer

Output parameter in normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register : 50h

Output parameter in abnormal completion

Register	7	6	5	4	3	2	1	0
Error	na					ABRT	na	
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Drive failure

Status register : 11h

Error register : 04h(Aborted Command)

(6) Idle Immediate (95h or E1h)

This device handles this command as NOP.

Input parameter

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Command	95h or E1h							

Device/Head register : Specifies the drive number

Output parameter in normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register : 50h

Output parameter in abnormal completion

Register	7	6	5	4	3	2	1	0
Error	na					ABRT	na	
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

[Drive failure]

Status register : 11h

Error register : 04h(Aborted Command)

(7) Initialize Drive Parameters (91h)

The host can specify the number of sectors per track (8 bits) and the number heads per cylinder (4 bits) by issuing this command. The drive is selected by DEV bit. This command does not check the validity of the numbers of sectors and heads. If they are invalid, an IDNF error is reported only when invalid access has been caused by other commands. When the number of cylinders calculated by the given parameter has exceeded the FFFFh, the parameter 54th word returned to the Identify Drive Information command returns FFFFh, and address conversion from CHS to LBA is calculated according to this value. This command can be executed even if DRDY bit is not set.

Input parameter

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	logical sector number per track							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	Max Head			
Command	91h							

Sector Count register : Number of sectors per traffic

Device/Head register : Specifies the drive number to the DEV bit, and sets the number of heads to the Head b3:0.

Output parameter in normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register : 50h (100 h when DRDY is not set)

Output parameter in abnormal completion

Register	7	6	5	4	3	2	1	0
Error	na					ABRT	na	
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Drive failure

Status register : 11h

Error register : 04h (Aborted Command)

(8) Recalibrate (1Xh)

This command is normally used to move the head arm of the hard disk drive unit to the cylinder 00h. In this device, it does not affect the operation. After completion of this command, the register value is initialized.

Input parameter

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na	LBA	na	DEV	na			
Command	1Xh							

Device/Head register : Specifies Drive number/LBA flag.

Output parameter in normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	CHS:01h/LBA:00h							
Cylinder Low	00h							
Cylinder High	00h							
Device/Head	na			DEV	na	0h		
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register : 50h

CHS mode
Sector Number register : 01h
Cylinder Low register : 00h
Cylinder High register : 00h
Head Register : 0h

LBA mode
Sector Number register : 00h
Cylinder Low register : 00h
Cylinder High register : 00h
Head Register : 0h

Output parameter in abnormal completion

Register	7	6	5	4	3	2	1	0
Error	na					ABRT	na	
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

[Drive failure]

Status register : 11h

Error register : 04h(Aborted Command)

(9) Read Buffer (E4h)

This command causes the host to read the data for one sector from the host buffer. Before this command is issued, it is necessary to use the Write Buffer command to write the sector data in the host buffer.

Input parameter

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Command	E4h							

Device/Head register : Specifies Drive number

Output parameter in normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register : 50h

Output parameter in abnormal completion

Register	7	6	5	4	3	2	1	0
Error	na					ABRT	na	
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Drive failure

Status register : 11h

Error register : 04h (Aborted Command)

(10) Read Multiple (C4h)

This command is the same as Read Sector(s) command, except that an interrupt occurs by each transfer of one block comprising the number of sectors defined by the Set Multiple command. In this device, however, the number of sectors per block, which can be set by the Set Multiple command, is only 1, so an interrupt occurs for each sector. However, when the nIEN is set ("1"), no interrupt takes place. Before this command is executed, it is necessary that execution of the Multiple command should be authorized by the Set Multiple command.

Input parameter

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
Sector Number	Sector number or LBA[7:0]							
Cylinder Low	Cylinder Low or LBA[15:8]							
Cylinder High	Cylinder High or LBA[23:16]							
Device/Head	na	LBA	na	DEV	Head or LBA[27:24]			
Command	C4h							

Sector Count register : Transfer of 256 sectors when the number of blocks to be read (= number of sectors) is 00h
Sector Number register : CHS: sector address/LBA: LBA[7:0]
Cylinder Low register : CHS: low-order cylinder address/LBA: LBA[15:8]
Cylinder High register : CHS: high-order cylinder address/LBA: LBA[23:16]
Device/Head register : CHS: head address/LBA: LBA [27:24], drive number and LBA flag

Output parameter in normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	Sector count							
Sector Number	Sector number or LBA[7:0]							
Cylinder Low	Cylinder Low or LBA[15:8]							
Cylinder High	Cylinder High or LBA[23:16]							
Device/Head	na			DEV	Head or LBA[27:24]			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register : 50h
Sector Count register : 00h
Sector Number register : Last read sector address (CHS: sector address/LBA: LBA [7:0])
Cylinder Low register : Last read sector address (CHS: low-order cylinder address/LBA: LBA [15:8])
Cylinder High register : Last read sector address (CHS: high-order cylinder address/LBA: LBA [23:16])
Device/Head register : Last read sector address (CHS: head address/LBA: LBA [27:24]) and drive number

Only when the error correction by ECC is executed, Status register b2 [CORR] is set. The Request Sense command return value in this case is 18h.

Output parameter in abnormal completion

Register	7	6	5	4	3	2	1	0
Error	BBK	UNC	MC	IDNF	MCR	ABRT	NM	AMNF
Sector Count	na							
Sector Number	Sector number or LBA[7:0]							
Cylinder Low	Cylinder Low or LBA[15:8]							
Cylinder High	Cylinder High or LBA[23:16]							
Device/Head	na			DEV	Head or LBA[27:24]			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

[Drive failure]
Status register : 11h
Error register : 04h(Aborted Command)

[Multiple disable]
Status register : 51h
Error register : 04h(Aborted Command)
Request Sense return value : 20h

[Address overflow]
Status register : 51h
Error register : 10h(ID Not Found)
Sector Count register : Number of remaining sectors to be transferred
Sector Number register : Address overflow (CHS: sector address/LBA: LBA [7:0])
Cylinder Low register : Address overflow (CHS: low-order cylinder address/LBA: LBA [15:8])
Cylinder High register : Address overflow (CHS: high-order cylinder address/LBA: LBA [23:16])
Device/Head register : Address overflow (CHS: head address/LBA: LBA [27:24]) and drive number
Request Sense return value : 2Fh

[Uncorrectable error]
(when an ECC uncorrectable error has occurred and 4 bits or more of 0s are present in the DS area)
Status register : 59h (51h after transfer of 512-byte data)
Error register : 40h(Uncorrectable Data Error)
Sector Count register : Number of remaining sectors to be transferred
Sector Number register : Address where an error has been detected (CHS: sector address/LBA: LBA [7:0])
Cylinder Low register : Address where an error has been detected (CHS: low-order cylinder address/LBA: LBA [15:8])
Cylinder High register : Address where an error has been detected (CHS: high-order cylinder address/LBA: LBA [23:16])
Device/Head register : Address where an error has been detected (CHS: head address/LBA: LBA [27:24]) and drive number
Request Sense return value : 11h

[Timeout error in read-out]
Status register : 51h
Error register : 04h(Command abort)
Sector Count register : Number of remaining sectors to be transferred
Sector Number register : Address where an error has been detected (CHS: sector address/LBA: LBA [7:0])
Cylinder Low register : Address where an error has been detected (CHS: low-order cylinder address/LBA: LBA [15:8])
Cylinder High register : Address where an error has been detected (CHS: high-order cylinder address/LBA: LBA [23:16])
Device/Head register : Address where an error has been detected (CHS: head address/LBA: LBA [27:24]) and drive number
Request Sense return value : 09h

[Timeout error during table creation]
Status register : 11h
Error register : 04h (Aborted command)

(11) Read Sector(s) (20h or 21h)

This command is used to read out the number of sectors specified in the Sector Count register from the sector number specified in Sector Number register. It can read from 1 to 256 sectors. When "00h" is set in the Sector Count register, it is regarded as transfer of data for 256 sectors, and is processed as such. This transfer starts from the sector specified in the Sector Number register. Independently of the presence and absence of an error, before data transfer DRQ is always set ("1"). Upon completion of the command, the cylinder, head and the sector number of last-read sector are specified in the task file register. The reading operation terminates at the sector where an error has occurred. The cylinder, head and sector number of the sector where an error has occurred are set in the task file register. Even when an ECC error has occurred, read-out data remains in the host buffer and the DRQ bit is set ("1").

Input parameter

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
Sector Number	Sector number or LBA[7:0]							
Cylinder Low	Cylinder Low or LBA[15:8]							
Cylinder High	Cylinder High or LBA[23:16]							
Device/Head	na	LBA	na	DEV	Head or LBA[27:24]			
Command	20h or 21h							

Sector Count register : 256 sectors are transferred when the number of sectors to be read out is 00h.
Sector Number register : CHS: sector address/LBA: LBA [7:0]
Cylinder Low register : CHS: low-order cylinder address/LBA: LBA [15:8]
Cylinder High register : CHS: high-order cylinder address/LBA: LBA [23:16]
Device/Head register : CHS: head address/LBA: LBA [27:24], drive number and LBA flag

Output parameter in normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	00h							
Sector Number	Sector number or LBA[7:0]							
Cylinder Low	Cylinder Low or LBA[15:8]							
Cylinder High	Cylinder High or LBA[23:16]							
Device/Head	na			DEV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register : 50h
Sector Count register : 00h
Sector Number register : Last-read sector address (CHS: sector address/LBA: LBA [7:0])
Cylinder Low register : Last-read sector address (CHS: low-order cylinder address/LBA: LBA [15:8])
Cylinder High register : Last-read sector address (CHS: high-order cylinder address/LBA: LBA [23:16])
Device/Head register : Last-read sector address (CHS: head address/LBA: LBA [27:24]) and, drive number

Only when the error correction by ECC is executed, Status register D2 [CORR] is set. The Request Sense command return value in this case is 18h.

Output parameter in abnormal completion

Register	7	6	5	4	3	2	1	0
Error	BBK	UNC	MC	IDNF	MCR	ABRT	NM	AMNF
Sector Count	rest sector count to complete cmd							
Sector Number	Sector number or LBA[7:0]							
Cylinder Low	Cylinder Low or LBA[15:8]							
Cylinder High	Cylinder High or LBA[23:16]							
Device/Head	na			DEV	Head or LBA[27:24]			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

[Drive failure]
Status register : 11h
Error register : 04h(Aborted Command)

[Address overflow]
Status register : 51h
Error register : 10h (ID Not Found)
Sector Count register : Number of remaining sectors to be transferred
Sector Number register : Address overflow (CHS: sector address/LBA: LBA [7:0])
Cylinder Low register : Address overflow (CHS: low-order cylinder address/LBA: LBA [15:8])
Cylinder High register : Address overflow (CHS: high-order cylinder address/LBA: LBA [23:16])
Device/Head register : Address overflow (CHS: head address/LBA: LBA [27:24]) and drive number
Request Sense return value : 2Fh

[Uncorrectable error]
(when an ECC uncorrectable error has occurred and 4 bits or more of 0s are present in the DS area)
Status register : 59h59h (51h after transfer of 512-byte data)
Error register : 40h(Uncorrectable Data Error)
Sector Count register : Number of remaining sectors to be transferred
Sector Number register : Address where an error has been detected (CHS: sector address/LBA: LBA [7:0])
Cylinder Low register : Address where an error has been detected (CHS: low-order cylinder address/LBA: LBA [15:8])
Cylinder High register : Address where an error has been detected (CHS: high-order cylinder address/LBA: LBA [23:16])
Device/Head register : Address where an error has been detected (CHS: head address/LBA: LBA [27:24]) and drive number
Request Sense return value : 11h

[Timeout error in read-out]
Status register : 51h
Error register : 04h(Command abort)
Sector Count register : Number of remaining sectors to be transferred
Sector Number register : Address where an error has been detected (CHS: sector address/LBA: LBA [7:0])
Cylinder Low register : Address where an error has been detected (CHS: low-order cylinder address/LBA: LBA [15:8])
Cylinder High register : Address where an error has been detected (CHS: high-order cylinder address/LBA: LBA [23:16])
Device/Head register : Address where an error has been detected (CHS: head address/LBA: LBA [27:24]) and drive number
Request Sense return value : 09h

[Timeout error during table creation]
Status register : 11h
Error register : 04h (Aborted command)

(12) Read Long Sector (22h or 23h)

Returns the ECC information where the user data of the requested sector and Write Long Sector command are added. Subsequent to user data transfer, ECC information comprising four bytes is read out. The ECC information after execution of this command for the sector where ECC information is not yet written is read as "FFFFFFFFh". In this device, only the transfer of one sector is supported. Despite the setting regarding the Long command setting of the Set Feature command, the number of bytes added to the ECC information in this command is fixed as four.

Input parameter

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
Sector Number	Sector number or LBA[7:0]							
Cylinder Low	Cylinder Low or LBA[15:8]							
Cylinder High	Cylinder High or LBA[23:16]							
Device/Head	na	LBA	na	DEV	Head or LBA[27:24]			
Command	22h or 23h							

Sector Count register : Number of sectors to be read out. Settable only in the case of 01h
Sector Number register : CHS: sector address/LBA: LBA [7:0]
Cylinder Low register : CHS: low-order cylinder address/LBA: LBA [15:8]
Cylinder High register : CHS: high-order cylinder address/LBA: LBA [23:16]
Device/Head register : CHS: head address/LBA: LBA [27:24], drive number and LBA flag

Output parameter in normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	00h							
Sector Number	Sector number or LBA[7:0]							
Cylinder Low	Cylinder Low or LBA[15:8]							
Cylinder High	Cylinder High or LBA[23:16]							
Device/Head	na			DEV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register : 50h
Sector Count register : 00h
Sector Number register : Read sector address (CHS: sector address/LBA: LBA [7:0])
Cylinder Low register : Read sector address (CHS: low-order cylinder address/LBA: LBA [15:8])
Cylinder High register : Read sector address (CHS: high-order cylinder address/LBA: LBA [23:16])
Device/Head register : Read sector address (CHS: head address/LBA: LBA [27:24]) and drive number

Output parameter in abnormal completion

Register	7	6	5	4	3	2	1	0
Error	BBK	UNC	MC	IDNF	MCR	ABRT	NM	AMNF
Sector Count	rest sector count to complete cmd							
Sector Number	Sector number or LBA[7:0]							
Cylinder Low	Cylinder Low or LBA[15:8]							
Cylinder High	Cylinder High or LBA[23:16]							
Device/Head	na			DEV	Head or LBA[27:24]			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

[Drive failure]
Status register : 11h
Error register : 04h(Aborted Command)

[Address overflow]
Status register : 51h
Error register : 10h(ID Not Found)
Sector Count register : 01h
Sector Number register : Address overflow (CHS: sector address/LBA: LBA [7:0])
Cylinder Low register : Address overflow (CHS: low-order cylinder address/LBA: LBA [15:8])
Cylinder High register : Address overflow (CHS: high-order cylinder address/LBA: LBA [23:16])
Device/Head register : Address overflow (CHS: head address/LBA: LBA [27:24]) and drive number
Request Sense return value : 2Fh

[Request to transfer multiple tasks]
Status register : 51h
Error register : 04h(Aborted Command)
Request Sense return value : 20h

[Timeout error in read-out]
Status register : 51h
Error register : 04h(Command abort)
Sector Count register : Number of remaining sectors
Sector Number register : Address overflow (CHS: sector address/LBA: LBA [7:0])
Cylinder Low register : Address overflow (CHS: low-order cylinder address/LBA: LBA [15:8])
Cylinder High register : Address overflow (CHS: high-order cylinder address/LBA: LBA [23:16])
Device/Head register : Address overflow (CHS: head address/LBA: LBA [27:24]) and drive number
Request Sense return value : 2Fh

[Timeout error during table creation]
Status register : 11h
Error register : 04h (Aborted command)

Note:
ECC information returned by this command is different from the ECC computation carried out inside the controller. In this command, ECC computation inside the device is not carried out. It should be noted, therefore that even when an uncorrectable error or correctable error has occurred, the error is not corrected or reported. Similarly, an error is not reported even when 4 bits or more of 0s are present in the DS area of the page where the requested sector is stored.

(13) Read Verify Sector (40h or 41h)

This command is the same as Read Sector(s) command, except that data are not sent to the host (DRQ bit is not set ("1")). Upon completion of this command, the cylinder and sector number of the last verified sector are set in the task file register. When an read-out error has occurred, verification terminates in the sector where an error has occurred. The cylinder and sector number of the sector where an error has occurred are set in the task file register. Furthermore, the number of sectors not yet verified is set in the Sector Count register.

Input parameter

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
Sector Number	Sector number or LBA[7:0]							
Cylinder Low	Cylinder Low or LBA[15:8]							
Cylinder High	Cylinder High or LBA[23:16]							
Device/Head	na	LBA	na	DEV	Head or LBA[27:24]			
Command	40h or 41h							

Sector Count register : 256 sectors are verified for 00h
Sector Number register : CHS: sector address/LBA: LBA [7:0]
Cylinder Low register : CHS: low-order cylinder address/LBA: LBA [15:8]
Cylinder High register : CHS: high-order cylinder address/LBA: LBA [23:16]
Device/Head register : CHS: head address/LBA: LBA [27:24], drive number and LBA flag

Output parameter in normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	00h							
Sector Number	Sector number or LBA[7:0]							
Cylinder Low	Cylinder Low or LBA[15:8]							
Cylinder High	Cylinder High or LBA[23:16]							
Device/Head	na			DEV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Sector Count register : 00h
Sector Number register : Last read sector address (CHS: sector address/LBA: LBA [7:0])
Cylinder Low register : Last read sector address (CHS: low-order cylinder address/LBA: LBA [15:8])
Cylinder High register : Last read sector address (CHS: high-order cylinder address/LBA: LBA [23:16])
Device/Head register : Last read sector address (CHS: head address/LBA: LBA [27:24]) and, drive number

Output parameter in abnormal completion

Register	7	6	5	4	3	2	1	0
Error	BBK	UNC	MC	IDNF	MCR	ABRT	NM	AMNF
Sector Count	rest sector count to verify							
Sector Number	Sector number or LBA[7:0]							
Cylinder Low	Cylinder Low or LBA[15:8]							
Cylinder High	Cylinder High or LBA[23:16]							
Device/Head	na			DEV	Head or LBA[27:24]			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Drive failure
Status register : 11h
Error register : 04h(Aborted Command)

[Address overflow]
Status register : 51h
Error register : 10h(ID Not Found)
Sector Count register : Number of sectors not verified
Sector Number register : Address overflow (CHS: sector address/LBA: LBA [7:0])
Cylinder Low register : Address overflow (CHS: low-order cylinder address/LBA: LBA [15:8])
Cylinder High register : Address overflow (CHS: high-order cylinder address/LBA: LBA [23:16])
Device/Head register : Address overflow (CHS: head address/LBA: LBA [27:24]) and drive number
Request Sense return value : 2Fh

[Uncorrectable error]
(when an ECC correctable error has occurred and 4 bits or more of 0s are present in the DS area)
Status register : 51h
Error register : 40h (Uncorrectable Data Error)
Sector Count register : Number of unverified sectors
Sector Number register : Address where an error has been detected (CHS: sector address/LBA: LBA [7:0])
Cylinder Low register : Address where an error has been detected (CHS: low-order cylinder address/LBA: LBA [15:8])
Cylinder High register : Address where an error has been detected (CHS: high-order cylinder address/LBA: LBA [23:16])
Device/Head register : Address where an error has been detected (CHS: head address/LBA: LBA [27:24]) and drive number
Request Sense return value : 11h

[Timeout error in read-out]
Status register : 51h
Error register : 04h(Command abort)
Sector Count register : Number of remaining sectors to be transferred
Sector Number register : Address where an error has been detected (CHS: sector address/LBA: LBA [7:0])
Cylinder Low register : Address where an error has been detected (CHS: low-order cylinder address/LBA: LBA [15:8])
Cylinder High register : Address where an error has been detected (CHS: high-order cylinder address/LBA: LBA [23:16])
Device/Head register : Address where an error has been detected (CHS: head address/LBA: LBA [27:24]) and drive number
Request Sense return value : 09h

[Timeout error during table creation]
Status register : 11h
Error register : 04h (Aborted command)

(14) Seek (7Xh)

This command is used to seek the track specified by the task file register. This device checks only the address to have been received and returns the results.

Input parameter

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	Sector number or LBA[7:0]							
Cylinder Low	Cylinder Low or LBA[15:8]							
Cylinder High	Cylinder High or LBA[23:16]							
Device/Head	na	LBA	na	DEV	Head or LBA[27:24]			
Command	7Xh							

Sector Number register : Sector for seek (CHS: sector address/LBA: LBA [7:0])
Cylinder Low register : Sector for seek (CHS: low-order cylinder address/LBA: LBA [15:8])
Cylinder High register : Sector for seek (CHS: high-order cylinder address/LBA: LBA [23:16])
Device/Head register : Sector for seek (CHS: head address/LBA: LBA [27:24]), drive number and LBA flag number

Output parameter in normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Sector Status register : 50h

Output parameter in abnormal completion

Register	7	6	5	4	3	2	1	0
Error	na		MC	IDNF	MCR	ABRT	NM	AMNF
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

[Drive failure]
Status register : 11h
Error register : 04h(Aborted Command)

[Address overflow]
Status register : 51h
Error register : 10h(ID Not Found)
Sector Number register : Address overflow (CHS: sector address/LBA: LBA [7:0])
Cylinder Low register : Address overflow (CHS: low-order cylinder address/LBA: LBA [15:8])
Cylinder High register : Address overflow (CHS: high-order cylinder address/LBA: LBA [23:16])
Device/Head register : Address overflow (CHS: head address/LBA: LBA [27:24]) and drive number
Request Sense return value : 2Fh

(15) Set Features(EFh)

This command is to change operation settings of this device.

For each of disable/Enable power level command, an error is returned as unsupported.

Feature		Operation
01h	support	Enable 8bit Data Transfer
09h	no	Enable Power Level 1 commands
55h	NOP	Disable Read Lock Ahead
66h	support	Disable Power on Reset establishment of defaults at Soft Reset
69h	NOP	NOP - Accepted for backward compatibility
81h	support	Disable 8bit Data Transfer
89h	no	Disable Power Level 1 commands
96h	NOP	NOP - Accepted for backward compatibility
97h	NOP	Accepted for backward compatibility
9Ah	NOP	NOP - Set the host current source capability
BBh	support	4bytes of data apply on Read/write Long commands
CCh	support	Enable Power on Reset establishment of defaults at Soft Reset

Eight-bit transfer upon turning on of power or after hardware reset is disabled.

Input parameter

Register	7	6	5	4	3	2	1	0
Features	Subcommand code							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Command	EFh							

Device/Head register : Specifies the drive number.

Feature Register : Function change parameter

(Values in the Sector Count register are not evaluated in this controller.)

Output parameter at normal completion

Sector Register : 50h

Output parameter in abnormal completion

Register	7	6	5	4	3	2	1	0
Error	na					ABRT	na	
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

[Drive failure]
Status register : 11h
Error register : 04h(Aborted Command)

[For unsupported parameters]
Status register : 51h
Error register : 04h(Aborted Command)
Request Sense return value : 20h

(16) Set Multiple Mode (C6h)

Read Multiple and Write Multiple operations are enabled by Set Multiple Mode command with number of block size for Multiple commands (number of sectors constituting blocks). This device supports only the specification of one sector per block. When the Sector Count register is 01h, the subsequent Read Multiple and Write Multiple commands are enabled. When the Sector Count register is 00h, the Read Multiple and Write Multiple commands are disabled. When other values are set, D0 (ABRT) of the Status register is set ("1"), and subsequent Multiple commands are disabled. When this command is processed normally, the preset value is reflected in the low-order bytes of the Identify Drive information word 59.

Input parameter

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector number per block							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Command	C6h							

Device/Head register : Specifies the drive number.
Sector Count register : Number of sectors per block (Only 00h or 01h is valid)

Output parameter in normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Sector Register : 50h

Output parameter in abnormal completion

Register	7	6	5	4	3	2	1	0
Error	na					ABRT	na	
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

[Drive failure]

Status register : 11h

Error register : 04h(Aborted Command)

[Number of unsupported block counts]

Status register : 51h

Error register : 04h(Aborted Command)

Request Sense return value : 09h

(17) Set Sleep Mode (99h or E6h)

This command places the drive into the sleep mode. This command allows the controller to clear BSY ("0"). When nIEN is cleared ("0"), an interrupt occurs and the mode is changed to the sleep mode. The interrupt is asserted for about 2 seconds. It is automatically negated if the Status register is not read during this period. After that, this device goes into the sleep mode. If the Status register is read during this period, the interrupt will be negated, and this device goes into the sleep mode.

Input parameter

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Command	99h or E6h							

Device/Head register : Specifies the drive number.

Output parameter in normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Sector Register : 10h

Output parameter in abnormal completion

Register	7	6	5	4	3	2	1	0
Error	na					ABRT	na	
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

[Drive failure]

Status register : 11h

Error register : 04h(Aborted Command)

(18) Standby (96h or E2h)

Response differs according to the operation mode of this device. Upon receipt of this command in the CF mode, the device immediately goes into the sleep mode, independently of the value of the Sector Count register. It does not affect the power down mode settings or time counts. In the SmartMedia™ mode, the device goes into the sleep mode after completing the same control as that of the Idle command.

Input parameter

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	CF:na/SmartMedia:Timer period value							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Command	96h or E2h							

Device/Head register : Specifies the drive number.

Sector Count register : Sets the automatic power down timer.

Output parameter in normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register : 50h

Output parameter in normal completion

Register	7	6	5	4	3	2	1	0
Error	na					ABRT	na	
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register : 11h

Error register : 04h (Aborted Command)

(19) Standby Immediate (94h or E0h)

Upon receipt of this command, the device immediately goes into the sleep mode.

Input parameter

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Command	E0h							

Device/Head register : Specifies the drive number.

Output parameter in normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register : 50h

Output parameter in abnormal completion

Register	7	6	5	4	3	2	1	0
Error	na					ABRT	na	
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register : 11h

Error register : 04h(Aborted Command)

(20) Write Buffer (E8h)

This command is used to rewrite the contents of the host buffer of this device into the pattern sent from the host. Upon receipt of this command, the device causes host buffer to be reset.

Input parameter

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Command	E8h							

Device/Head register

Output parameter in normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register : 50h

Output parameter in abnormal completion

Register	7	6	5	4	3	2	1	0
Error	na					ABRT	na	
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DEV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register : 11h

Error register : 04h (Aborted Command)

(21) Write Multiple (C5h)

This device supports only one sector in terms of block counts which can be set by the Set Multiple command. So the operation is the same as that of the Write Sector(s) command.

Input parameter

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
Sector Number	Sector number or LBA[7:0]							
Cylinder Low	Cylinder Low or LBA[15:8]							
Cylinder High	Cylinder High or LBA[23:16]							
Device/Head	na	LBA	na	DEV	Head or LBA[27:24]			

Sector Count register : Number of sectors to be written (256 sectors transferred in the case of 00h)
Sector Number register : CHS : Sector address to be formatted LBA (7:0)
Cylinder Low register : CHS : low-order cylinder address/LBA: LBA [15:8])
Cylinder High register : CHS : high-order cylinder address/LBA: LBA [23:16])
Device/Head register : CHS : head address/LBA: LBA [27:24]), drive number and LBA flag number

Output parameter in normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	00h							
Sector Number	Sector number or LBA[7:0]							
Cylinder Low	Cylinder Low or LBA[15:8]							
Cylinder High	Cylinder High or LBA[23:16]							
Device/Head	na			DEV	Head or LBA[27:24]			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register : 50h
Sector Count register : 00h
Sector Number register : Last written sector address CHS : Sector address to be formatted LBA (7:0)
Cylinder Low register : Last written sector address CHS : low-order cylinder address/LBA: LBA [15:8])
Cylinder High register : Last written sector address CHS : high-order cylinder address/LBA: LBA [23:16])
Device/Head register : Last written sector address (CHS: head address/LBA: LBA [27:24]) and drive number

Output parameter in abnormal completion

Register	7	6	5	4	3	2	1	0
Error	BBK	WP	MC	IDNF	MCR	ABRT	NM	AMNF
Sector Count	rest sector count to write							
Sector Number	Sector number or LBA[7:0]							
Cylinder Low	Cylinder Low or LBA[15:8]							
Cylinder High	Cylinder High or LBA[23:16]							
Device/Head	na			DEV	Head or LBA[27:24]			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

[Drive failure]
Status register : 11h
Error register : 04h(Aborted Command)

[Multiple disable]
Status register : 51h
Error register : 04h(Aborted Command)
Request Sense return value : 20h

[Address overflow]

Status register	: 51h
Error register	: 10h(ID Not Found)
Sector Count register	: Number of remaining sectors to be transferred
Sector Number register	: Address overflow CHS : Sector address to be formatted LBA (7:0)
Cylinder Low register	: Address overflow CHS : low-order cylinder address/LBA: LBA [15:8])
Cylinder High register	: Address overflow CHS : high-order cylinder address/LBA: LBA [23:16])
Device/Head register	: Address overflow(CHS: head address/LBA: LBA [27:24]) and drive number
Request Sense return value	: 2Fh

[No empty block]

Status register	: 71hDWF Assert
Error register	: 04h(Abort Command)
Sector Count register	: Number of remaining sectors to be transferred
Sector Number register	: Address where a write error has occurred CHS : Sector address to be formatted LBA (7:0)
Cylinder Low register	: Address where a write error has occurred CHS : low-order cylinder address/LBA: LBA [15:8])
Cylinder High register	: Address where a write error has occurred CHS : high-order cylinder address/LBA: LBA [23:16])
Device/Head register	: Address where a write error has occurred(CHS: head address/LBA: LBA [27:24]) and drive number
Request Sense return value	: 3Ah

[Timeout in writing]

Status register	: 71h(31h, when an error has occurred in writing and an error has also occurred in immediately preceding writing and erasure)
Error register	: 04h (Abort)
Sector Count register	: Number of sectors unable to be formatted
Sector Number register	: Sector address where time has expired for writing LBA[7:0]
Cylinder Low register	: Sector address where time has expired for writing LBA[15:8]
Cylinder High register	: Sector address where time has expired for writing LBA[23:16]
Device/Head register	: Sector address where time has expired for writing LBA[27:24]
Request Sense return value	: 03h

[Write/erase status error](Erase status error occurs only in the case of "Foh" write failure in the redundant part.)

Status register	:71h(31h, when an error has occurred in writing and an error has also occurred in immediately preceding writing and erasure)
Error register	: 80h (Bad block)
Sector Count register	: Number of sectors unable to be formatted
Sector Number register	: Sector address where status error has occurred LBA[7:0]
Cylinder Low register	: Sector address where status error has occurred LBA[15:8]
Cylinder High register	: Sector address where status error has occurred LBA[23:16]
Device/Head register	: Sector address where status error has occurred LBA[27:24]
Request Sense return value	: 03h

[Write protect error] (When the SmartMedia™ is set to the write protect status, and when the specification is designed for Mask ROM)

Status register	: 71h
Error register	: 40h (Write protected)
Request Sense return value	: 03h

[Timeout error during table creation]

Status register	: 11h
Error register	: 04h (Aborted command)

[Physical block inspection error]
Status register : 71h
Error register : 04h (Aborted Command)
Request Sense return value : 0Ch

(22) Write Sector(s) (30h or 31h)

This command is used to write the number of sectors specified in the Sector Count register from the sector number specified in the Sector Number register. When “00h” is set to the Sector Count register, it is regarded as transfer of data for 256 sectors, and is processed as such. Upon completion of the command, the cylinder, head and sector number of the last written sector are specified in the task file register. When a write error has occurred, the contents of the task file register are not always the address where an error has occurred.

Input parameter

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
Sector Number	Sector number or LBA[7:0]							
Cylinder Low	Cylinder Low or LBA[15:8]							
Cylinder High	Cylinder High or LBA[23:16]							
Device/Head	na	LBA	na	DEV	Head or LBA[27:24]			
Command	30h or 31h							

Sector Count register : Number of sectors to be written (256 sectors transferred in the case of 00h)
Sector Number register : CHS : Sector address to be formatted LBA (7:0)
Cylinder Low register : CHS : low-order cylinder address/LBA: LBA [15:8])
Cylinder High register : CHS : high-order cylinder address/LBA: LBA [23:16])
Device/Head register : CHS : head address/LBA: LBA [27:24]), drive number and LBA flag number

Output parameter in normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	00h							
Sector Number	Sector number or LBA[7:0]							
Cylinder Low	Cylinder Low or LBA[15:8]							
Cylinder High	Cylinder High or LBA[23:16]							
Device/Head	na			DEV	Head or LBA[27:24]			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register : 50h
Sector Count register : 00h
Sector Number register : Last written sector address CHS : Sector address to be formatted LBA (7:0)
Cylinder Low register : Last written sector address CHS : low-order cylinder address/LBA: LBA [15:8])
Cylinder High register : Last written sector address CHS : high-order cylinder address/LBA: LBA [23:16])
Device/Head register : Last written sector address (CHS: head address/LBA: LBA [27:24]) and drive number

Output parameter in abnormal completion

Register	7	6	5	4	3	2	1	0
Error	BBK	WP	MC	IDNF	MCR	ABRT	NM	AMNF
Sector Count	rest sector count to write							
Sector Number	Sector number or LBA[7:0]							
Cylinder Low	Cylinder Low or LBA[15:8]							
Cylinder High	Cylinder High or LBA[23:16]							
Device/Head	na			DEV	Head or LBA[27:24]			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

[Drive failure]
Status register : 11h
Error register : 04h(Aborted Command)

[Address overflow]
Status register : 51h
Error register : 10h(ID Not Found)
Sector Count register : Number of remaining sectors to be transferred
Sector Number register : Address overflow CHS : Sector address to be formatted LBA (7:0)
Cylinder Low register : Address overflow CHS : low-order cylinder address/LBA: LBA [15:8])
Cylinder High register : Address overflow CHS : high-order cylinder address/LBA: LBA [23:16])
Device/Head register : Address overflow(CHS: head address/LBA: LBA [27:24]) and drive number
Request Sense return value : 2Fh

[No empty block]
Status register : 71h DWF Assert
Error register : 04h(Abort Command)
Sector Count register : Number of remaining sectors to be transferred
Sector Number register : Address where a write error has occurred CHS : Sector address to be formatted LBA (7:0)
Cylinder Low register : Address where a write error has occurred CHS : low-order cylinder address/LBA: LBA [15:8])
Cylinder High register : Address where a write error has occurred CHS : high-order cylinder address/LBA: LBA [23:16])
Device/Head register : Address where a write error has occurred(CHS: head address/LBA: LBA [27:24]) and drive number
Request Sense return value : 3Ah

[Timeout in writing]
Status register : 71h(31h, when an error has occurred in writing and an error has also occurred in immediately preceding writing and erasure)
Error register : 04h (Abort)
Sector Count register : Number of sectors unable to be formatted
Sector Number register : Sector address where time has expired for writing LBA[7:0]
Cylinder Low register : Sector address where time has expired for writing LBA[15:8]
Cylinder High register : Sector address where time has expired for writing LBA[23:16]
Device/Head register : Sector address where time has expired for writing LBA[27:24]
Request Sense return value : 03h

[Write/erase status error](Erase status error occurs only in the case of "Foh" write failure in the redundant part.)

Status register : 71h(31h, when an error has occurred in writing and an error has also occurred in immediately preceding writing and erasure)
Error register : 80h (Bad block)
Sector Count register : Number of sectors unable to be formatted
Sector Number register : Sector address where status error has occurred LBA[7:0]
Cylinder Low register : Sector address where status error has occurred LBA[15:8]
Cylinder High register : Sector address where status error has occurred LBA[23:16]
Device/Head register : Sector address where status error has occurred LBA[27:24]
Request Sense return value : 03h

[Write protect error](When the SmartMedia™ is set to the write protect status, and when the specification is designed for Mask ROM)

Status register : 71h
Error register : 40h (Write protected)
Request Sense return value : 03h

[Timeout error during table creation]

Status register : 11h
Error register : 04h (Aborted command)

[Physical block inspection error]

Status register : 71h
Error register : 04h (Aborted Command)
Request Sense return value : 0Ch

(23) Write Long Sector (32h or 33h)

This command is used to write the sector data and ECC information for Long command directly from the sector buffer. The ECC information is four bytes long. It is normally at the end of the 512 bytes of sector data, and is sent from the host. This command supports only one sector transfer. Independently of the settings of the LONG command or sub-command of the Set Feature commands, ECC information of this command is 4 bytes long.

Input parameter

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
Sector Number	Sector number or LBA[7:0]							
Cylinder Low	Cylinder Low or LBA[15:8]							
Cylinder High	Cylinder High or LBA[23:16]							
Device/Head	na	LBA	na	DEV	Head or LBA[27:24]			
Command	32h or 33h							

Sector Count register : Number of sectors to be written. Settable only in the case of 01h
Sector Number register : CHS : Sector address to be formatted LBA (7:0)
Cylinder Low register : CHS : low-order cylinder address/LBA: LBA [15:8])
Cylinder High register : CHS : high-order cylinder address/LBA: LBA [23:16])
Device/Head register : CHS : head address/LBA: LBA [27:24]), drive number and LBA flag number

Output parameter in normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	00h							
Sector Number	Sector number or LBA[7:0]							
Cylinder Low	Cylinder Low or LBA[15:8]							
Cylinder High	Cylinder High or LBA[23:16]							
Device/Head	na			DEV	Head or LBA[27:24]			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register : 50h
Sector Count register : 00h
Sector Number register : Last written sector address CHS : Sector address to be formatted LBA (7:0)
Cylinder Low register : Last written sector address CHS : low-order cylinder address/LBA: LBA [15:8])
Cylinder High register : Last written sector address CHS : high-order cylinder address/LBA: LBA [23:16])
Device/Head register : Last written sector address (CHS: head address/LBA: LBA [27:24]) and drive number

Output parameter in abnormal completion

Register	7	6	5	4	3	2	1	0
Error	BBK	WP	MC	IDNF	MCR	ABRT	NM	AMNF
Sector Count	rest sector count to write							
Sector Number	Sector number or LBA[7:0]							
Cylinder Low	Cylinder Low or LBA[15:8]							
Cylinder High	Cylinder High or LBA[23:16]							
Device/Head	na			DEV	Head or LBA[27:24]			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

[Drive failure]
Status register : 11h
Error register : 04h(Aborted Command)

[Multiple sector transfer request]
Status register : 51h
Error register : 04h(Aborted Command)
Request Sense return value : 20h

[Address overflow]
Status register : 51h
Error register : 10h(ID Not Found)
Sector Count register : Number of remaining sectors to be transferred
Sector Number register : Address overflow CHS : Sector address to be formatted LBA (7:0)
Cylinder Low register : Address overflow CHS : low-order cylinder address/LBA: LBA [15:8])
Cylinder High register : Address overflow CHS : high-order cylinder address/LBA: LBA [23:16])
Device/Head register : Address overflow(CHS: head address/LBA: LBA [27:24]) and drive number
Request Sense return value : 2Fh

[No empty block]

Status register	: 71h DWF Assert
Error register	: 04h(Abort Command)
Sector Count register	: Number of remaining sectors to be transferred
Sector Number register	: Address where a write error has occurred CHS : Sector address to be formatted LBA (7:0)
Cylinder Low register	: Address where a write error has occurred CHS : low-order cylinder address/LBA: LBA [15:8])
Cylinder High register	: Address where a write error has occurred CHS : high-order cylinder address/LBA: LBA [23:16])
Device/Head register	: Address where a write error has occurred(CHS: head address/LBA: LBA [27:24]) and drive number
Request Sense return value	: 3Ah

[Timeout in writing]

Status register	: 71h(31h, when an error has occurred in writing and an error has also occurred in immediately preceding writing and erasure)
Error register	: 04h (Abort)
Sector Count register	: Number of sectors unable to be formatted
Sector Number register	: Sector address where time has expired for writing LBA[7:0]
Cylinder Low register	: Sector address where time has expired for writing LBA[15:8]
Cylinder High register	: Sector address where time has expired for writing LBA[23:16]
Device/Head register	: Sector address where time has expired for writing LBA[27:24]
Request Sense return value	: 03h

[Write/erase status error](Erase status error occurs only in the case of "Foh" write failure in the redundant part.)

Status register	: 71h(31h, when an error has occurred in writing and an error has also occurred in immediately preceding writing and erasure)
Error register	: 80h (Bad block)
Sector Count register	: Number of sectors unable to be formatted
Sector Number register	: Sector address where status error has occurred LBA[7:0]
Cylinder Low register	: Sector address where status error has occurred LBA[15:8]
Cylinder High register	: Sector address where status error has occurred LBA[23:16]
Device/Head register	: Sector address where status error has occurred LBA[27:24]
Request Sense return value	: 03h

[Write protect error](When the SmartMedia™ is set to the write protect status, and when the specification is designed for Mask ROM)

Status register	: 71h
Error register	: 40h (Write protected)
Request Sense return value	: 03h

[Timeout error during table creation]

Status register	: 11h
Error register	: 04h (Aborted command)

[Physical block inspection error]

Status register	: 71h
Error register	: 04h(Aborted Command)
Request Sense return value	: 0Ch

(24) Write Verify (3Ch)

After programming the flash memory, this command reads out the programmed sector to check read error (uncorrectable error). When an uncorrectable error has occurred, the command is aborted. Even when a correctable error has occurred, correction of the flash memory is not carried out.

Input parameter

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
Sector Number	Sector number or LBA[7:0]							
Cylinder Low	Cylinder Low or LBA[15:8]							
Cylinder High	Cylinder High or LBA[23:16]							
Device/Head	na	LBA	na	DEV	Head or LBA[27:24]			
Command	3Ch							

Sector Count register : Number of sectors to be written (256 sectors transferred in the case of 00h)
Sector Number register : CHS : Sector address to be formatted LBA (7:0)
Cylinder Low register : CHS : low-order cylinder address/LBA: LBA [15:8])
Cylinder High register : CHS : high-order cylinder address/LBA: LBA [23:16])
Device/Head register : CHS : head address/LBA: LBA [27:24]), drive number and LBA flag number

Output parameter in normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	00h							
Sector Number	Sector number or LBA[7:0]							
Cylinder Low	Cylinder Low or LBA[15:8]							
Cylinder High	Cylinder High or LBA[23:16]							
Device/Head	na			DEV	Head or LBA[27:24]			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register : 50h
Sector Count register : 00h
Sector Number register : Last written sector address CHS : Sector address to be formatted LBA (7:0)
Cylinder Low register : Last written sector address CHS : low-order cylinder address/LBA: LBA [15:8])
Cylinder High register : Last written sector address CHS : high-order cylinder address/LBA: LBA [23:16])
Device/Head register : Last written sector address (CHS: head address/LBA: LBA [27:24]) and drive number

Output parameter in abnormal completion

Register	7	6	5	4	3	2	1	0
Error	BBK	WP	MC	IDNF	MCR	ABRT	NM	AMNF
Sector Count	rest sector count to write							
Sector Number	Sector number or LBA[7:0]							
Cylinder Low	Cylinder Low or LBA[15:8]							
Cylinder High	Cylinder High or LBA[23:16]							
Device/Head	na			DEV	Head or LBA[27:24]			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

[Drive failure]
Status register : 11h
Error register : 04h(Aborted Command)

[Address overflow]

Status register	: 51h
Error register	: 10h(ID Not Found)
Sector Count register	: Number of remaining sectors to be transferred
Sector Number register	: Address overflow CHS : Sector address to be formatted LBA (7:0)
Cylinder Low register	: Address overflow CHS : low-order cylinder address/LBA: LBA [15:8])
Cylinder High register	: Address overflow CHS : high-order cylinder address/LBA: LBA [23:16])
Device/Head register	: Address overflow(CHS: head address/LBA: LBA [27:24]) and drive number
Request Sense return value	: 2Fh

[No empty block]

Status register	: 71h DWF Assert
Error register	: 04h(Abort Command)
Sector Count register	: Number of remaining sectors to be transferred
Sector Number register	: Address where a write error has occurred CHS : Sector address to be formatted LBA (7:0)
Cylinder Low register	: Address where a write error has occurred CHS : low-order cylinder address/LBA: LBA [15:8])
Cylinder High register	: Address where a write error has occurred CHS : high-order cylinder address/LBA: LBA [23:16])
Device/Head register	: Address where a write error has occurred(CHS: head address/LBA: LBA [27:24]) and drive number
Request Sense return value	: 3Ah

[Uncorrectable error] (When an ECC correctable error has occurred and 4 bits or more of 0s are detected in the DS area.)

Status register	: 51h
Error register	: 40h(Uncorrectable Data Error / Write Protected)
Sector Count register	: Number of remaining sectors to be transferred
Sector Number register	: Address where an error has been detected CHS : Sector address to be formatted LBA (7:0)
Cylinder Low register	: Address where an error has been detected CHS : low-order cylinder address/LBA: LBA [15:8])
Cylinder High register	: Address where an error has been detected CHS : high-order cylinder address/LBA: LBA [23:16])
Device/Head register	: Address where an error has been detected(CHS: head address/LBA: LBA [27:24]) and drive number
Request Sense return value	: 11h

[Timeout in writing]

Status register	: 71h(31h, when an error has occurred in writing and an error has also occurred in immediately preceding writing and erasure)
Error register	: 04h (Abort)
Sector Count register	: Number of sectors unable to be formatted
Sector Number register	: Sector address where time has expired for writing LBA[7:0]
Cylinder Low register	: Sector address where time has expired for writing LBA[15:8]
Cylinder High register	: Sector address where time has expired for writing LBA[23:16]
Device/Head register	: Sector address where time has expired for writing LBA[27:24]
Request Sense return value	: 03h

[Write/erase status error](Erase status error occurs only in the case of "Foh" write failure in the redundant part.)

Status register	: 71h(31h, when an error has occurred in writing and an error has also occurred in immediately preceding writing and erasure)
Error register	: 80h (Bad block)
Sector Count register	: Number of sectors unable to be formatted
Sector Number register	: Sector address where status error has occurred LBA[7:0]
Cylinder Low register	: Sector address where status error has occurred LBA[15:8]
Cylinder High register	: Sector address where status error has occurred LBA[23:16]
Device/Head register	: Sector address where status error has occurred LBA[27:24]
Request Sense return value	: 03h

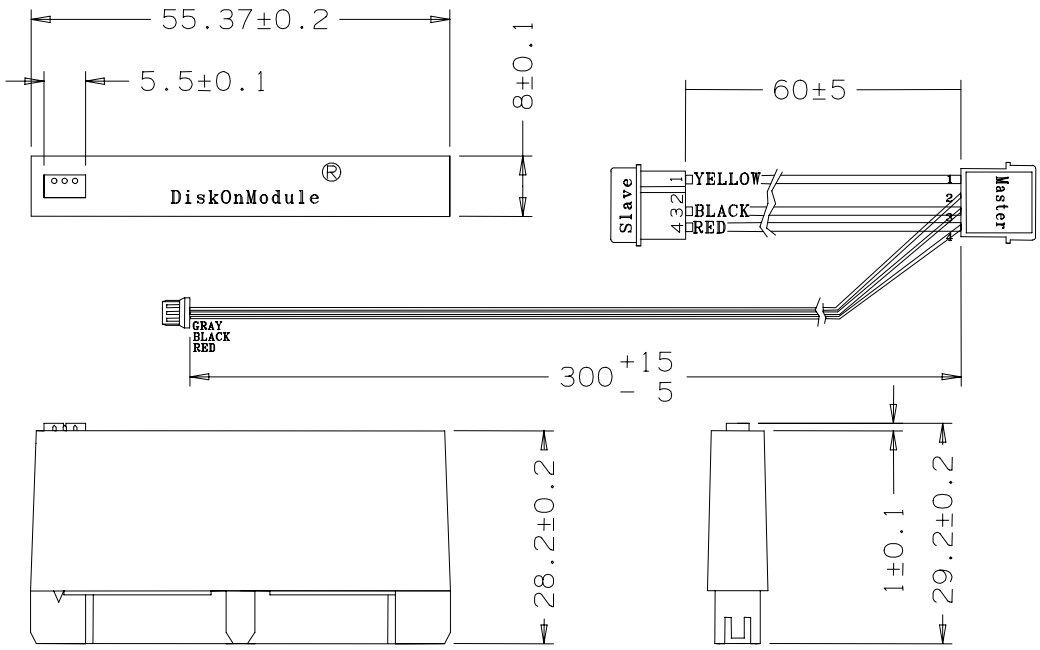
[Write protect error] (When the SmartMedia™ is set to the write protect status, and when the specification is designed for Mask ROM)
Status register : 71h
Error register : 40h (Write protected)
Request Sense return value : 03h

[Timeout error during table creation]
Status register : 11h
Error register : 04h (Aborted command)

[Physical block inspection error]
Status register : 71h
Error register : 04h (Aborted Command)
Request Sense return value : 0Ch

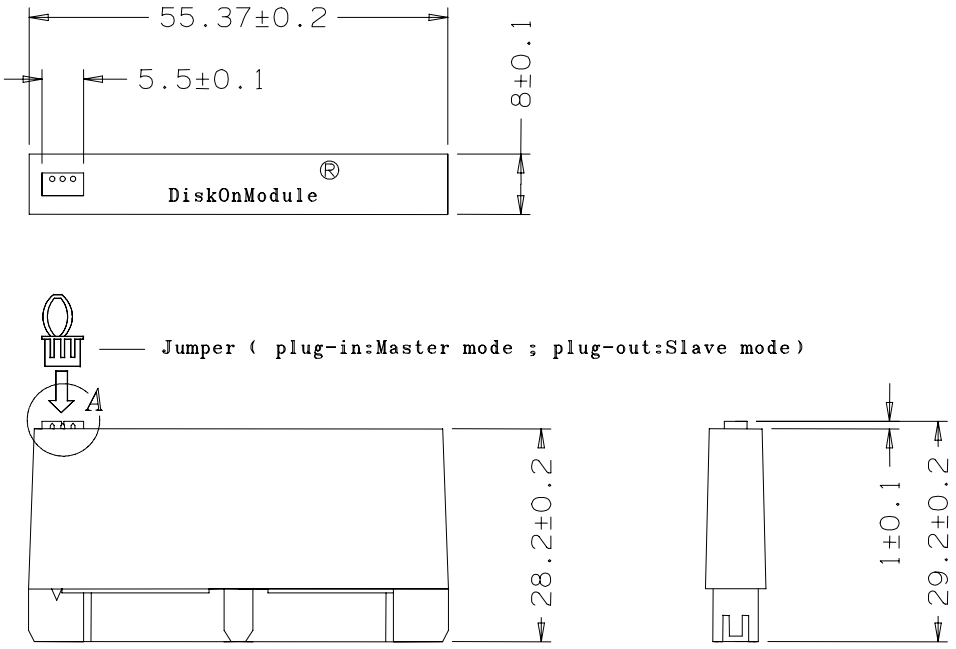
Physical Outline

FDXXX-019P.XD4



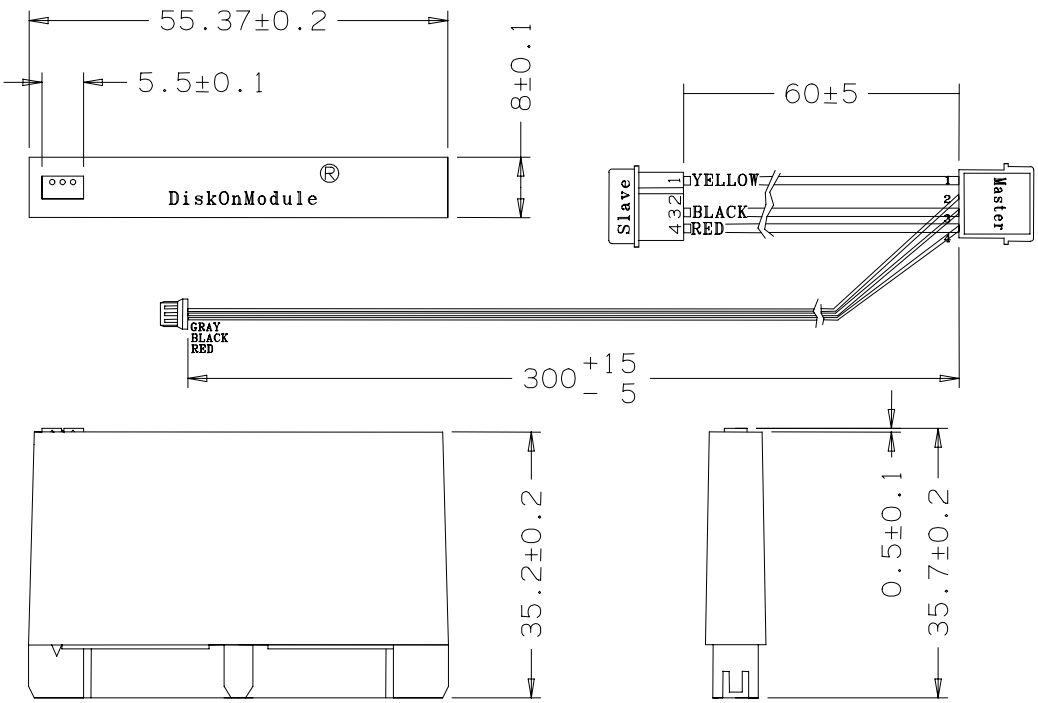
Physical Outline

FDXXX-019PR.XD4



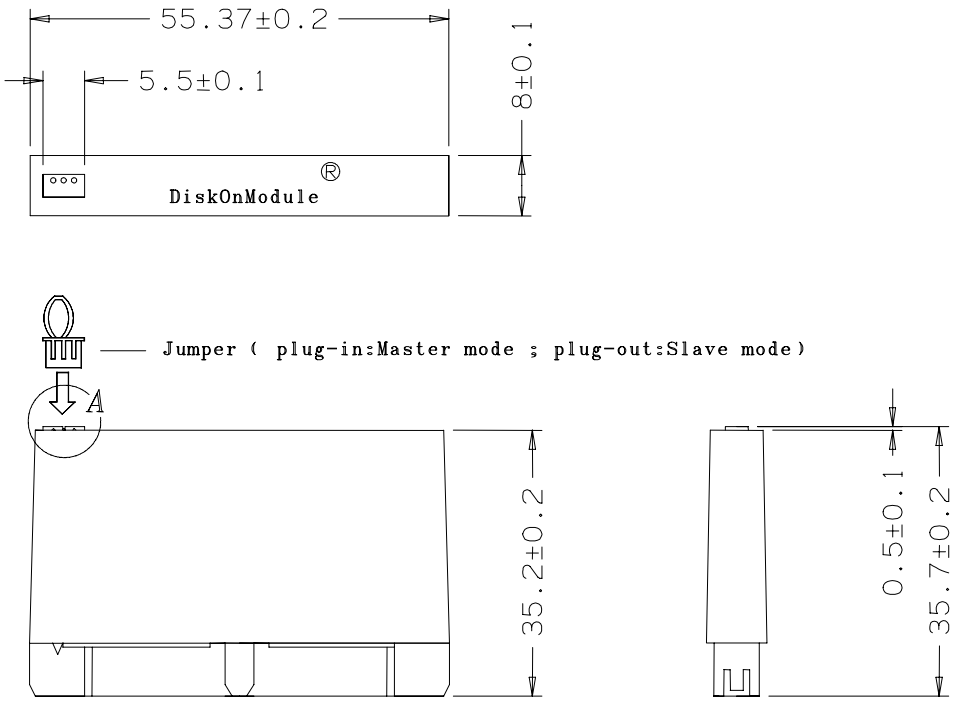
Physical Outline

FDXXX-026P.XD4



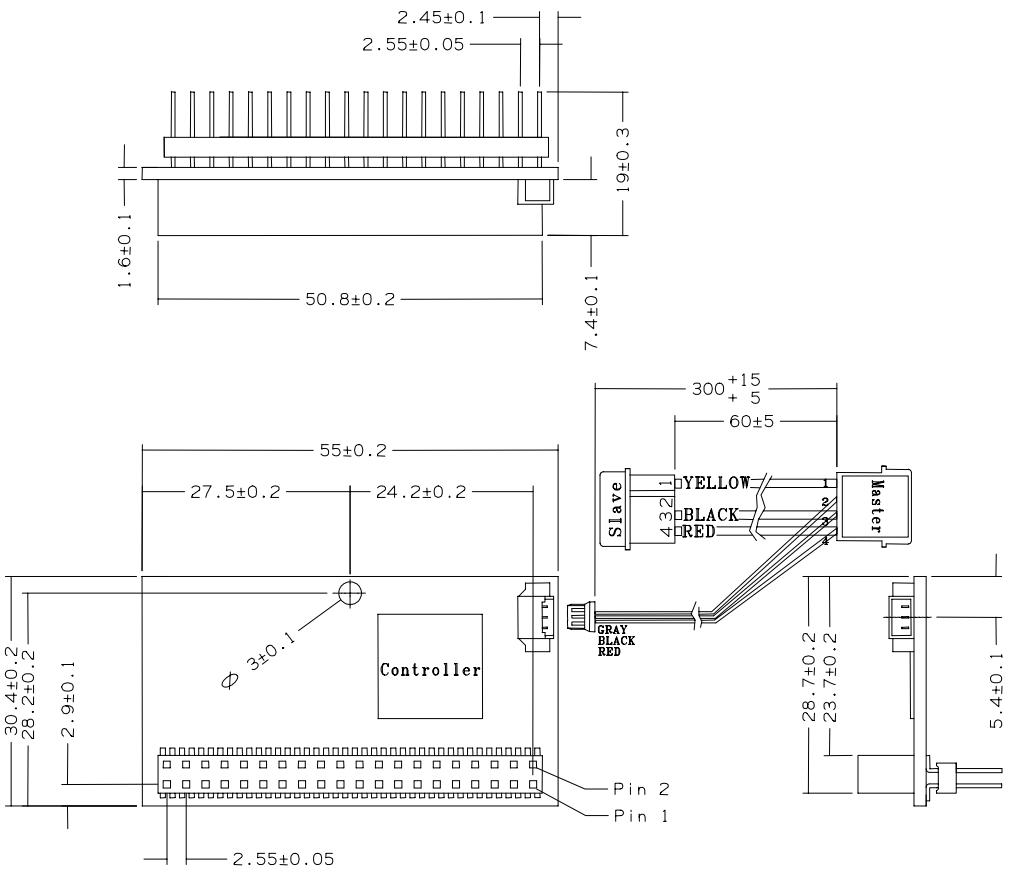
Physical Outline

FDXXX-026PR.XD4



Physical Outline

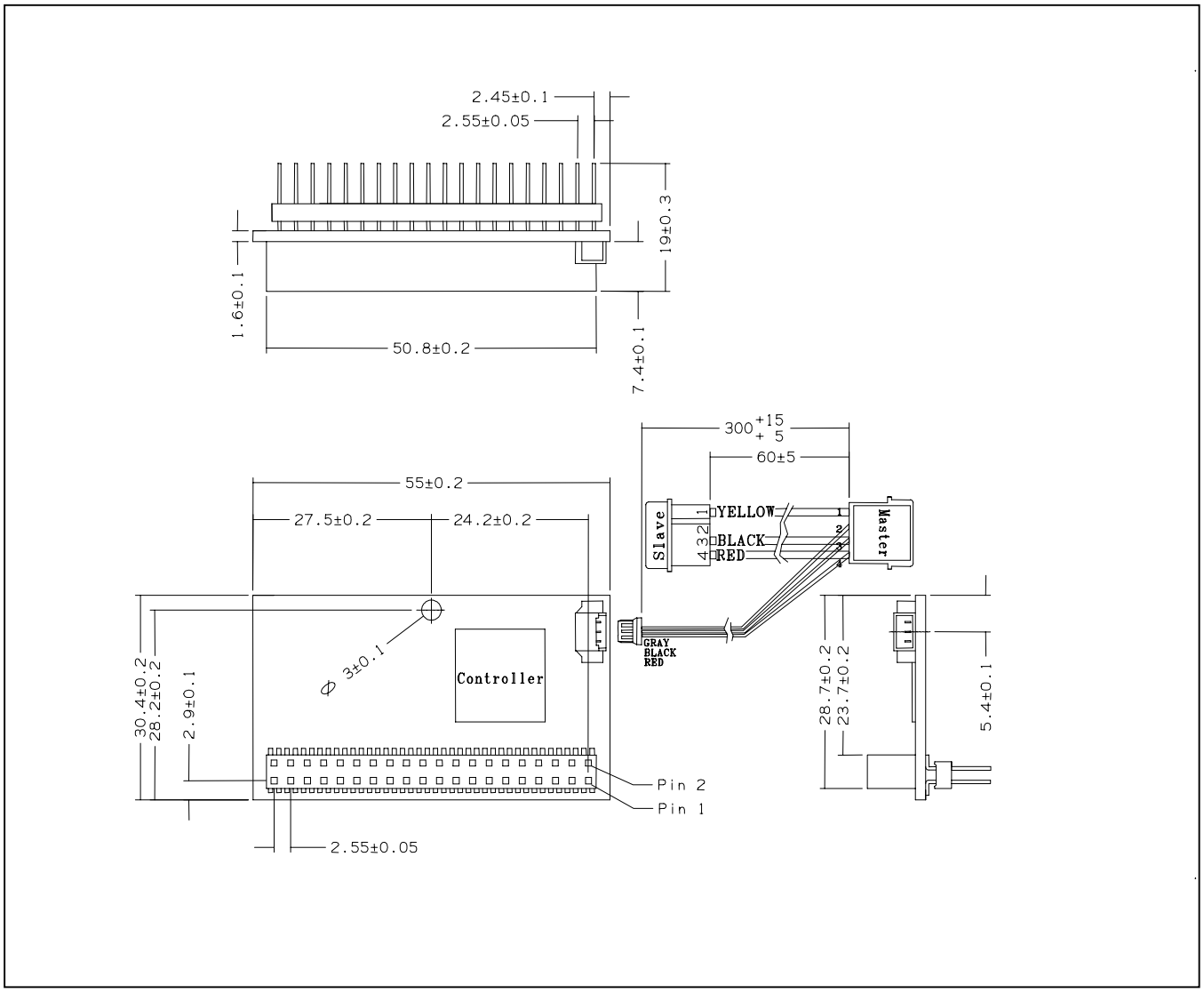
FDXXX-030LXX.XD4



Product Number	Controller Side Connector	Firmware Side Connector
FDXXX-030LMM.XD4	Male	Male
FDXXX-030LMF.XD4	Male	Female
FDXXX-030LMD.XD4	Male	×
FDXXX-030LFM.XD4	Female	Male
FDXXX-030LFF.XD4	Female	Female
FDXXX-030LFD.XD4	Female	×
FDXXX-030LDM.XD4	×	Male
FDXXX-030LDF.XD4	×	Female

Physical Outline

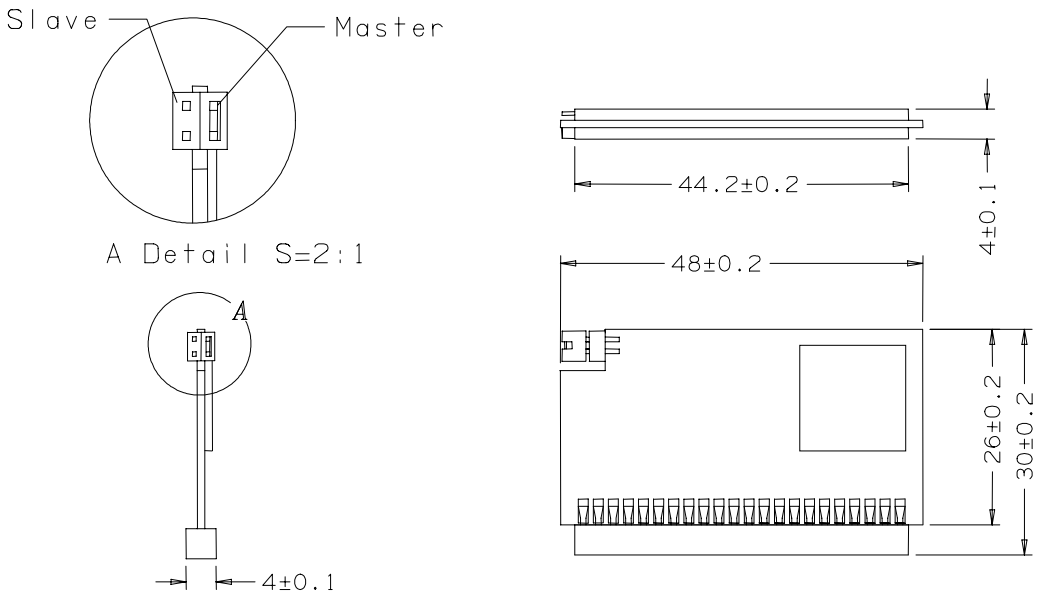
FDXXX-030LXXR.XD4



Product Number	Controller Side Connector	Firmware Side Connector
FDXXX-030LMMR.XD4	Male	Male
FDXXX-030LMFR.XD4	Male	Female
FDXXX-030LMDR.XD4	Male	×
FDXXX-030LFMR.XD4	Female	Male
FDXXX-030LFFR.XD4	Female	Female
FDXXX-030LFDR.XD4	Female	×
FDXXX-030LDMR.XD4	×	Male
FDXXX-030LDFR.XD4	×	Female

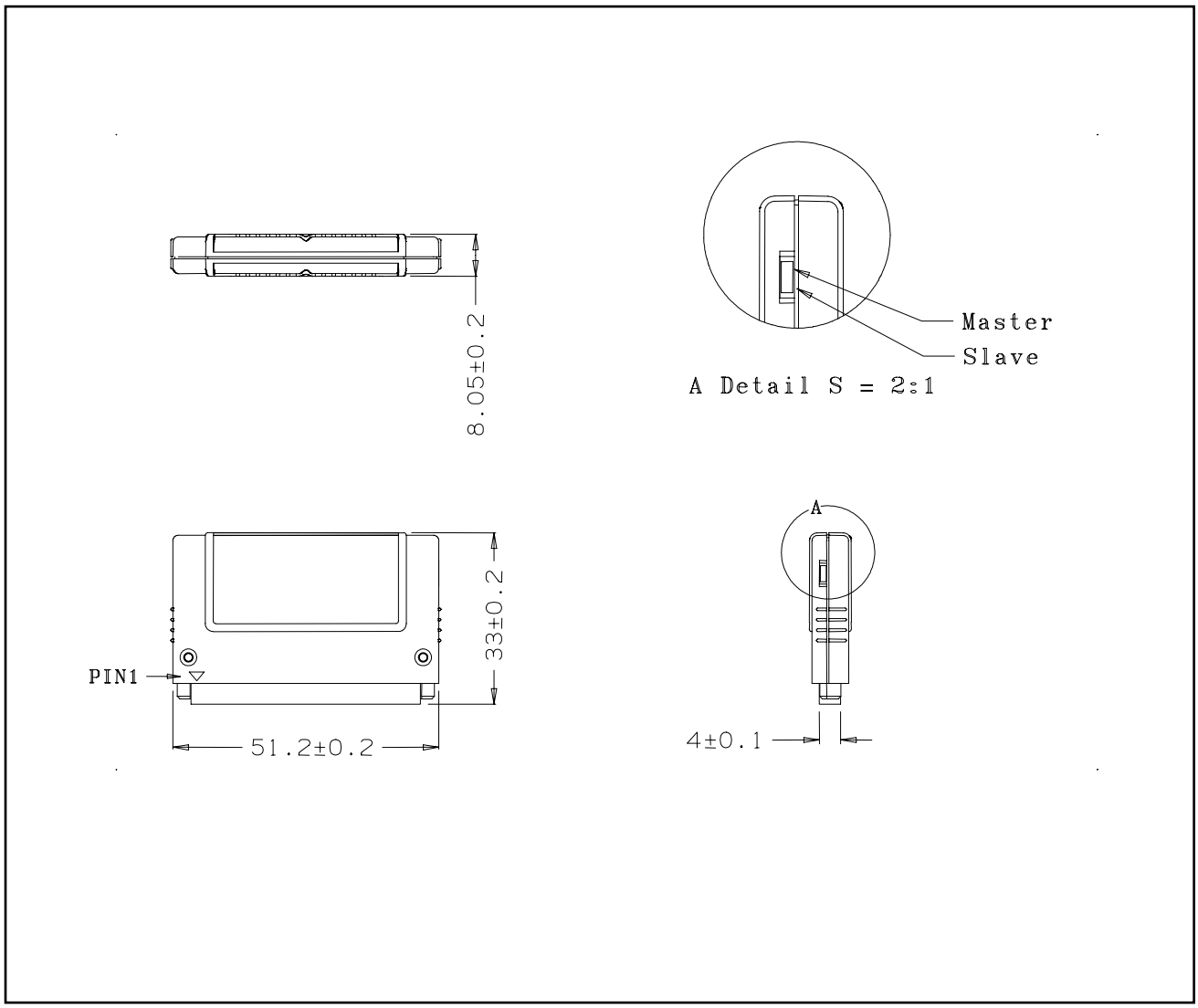
Physical Outline

FDXXX-426P.XD4



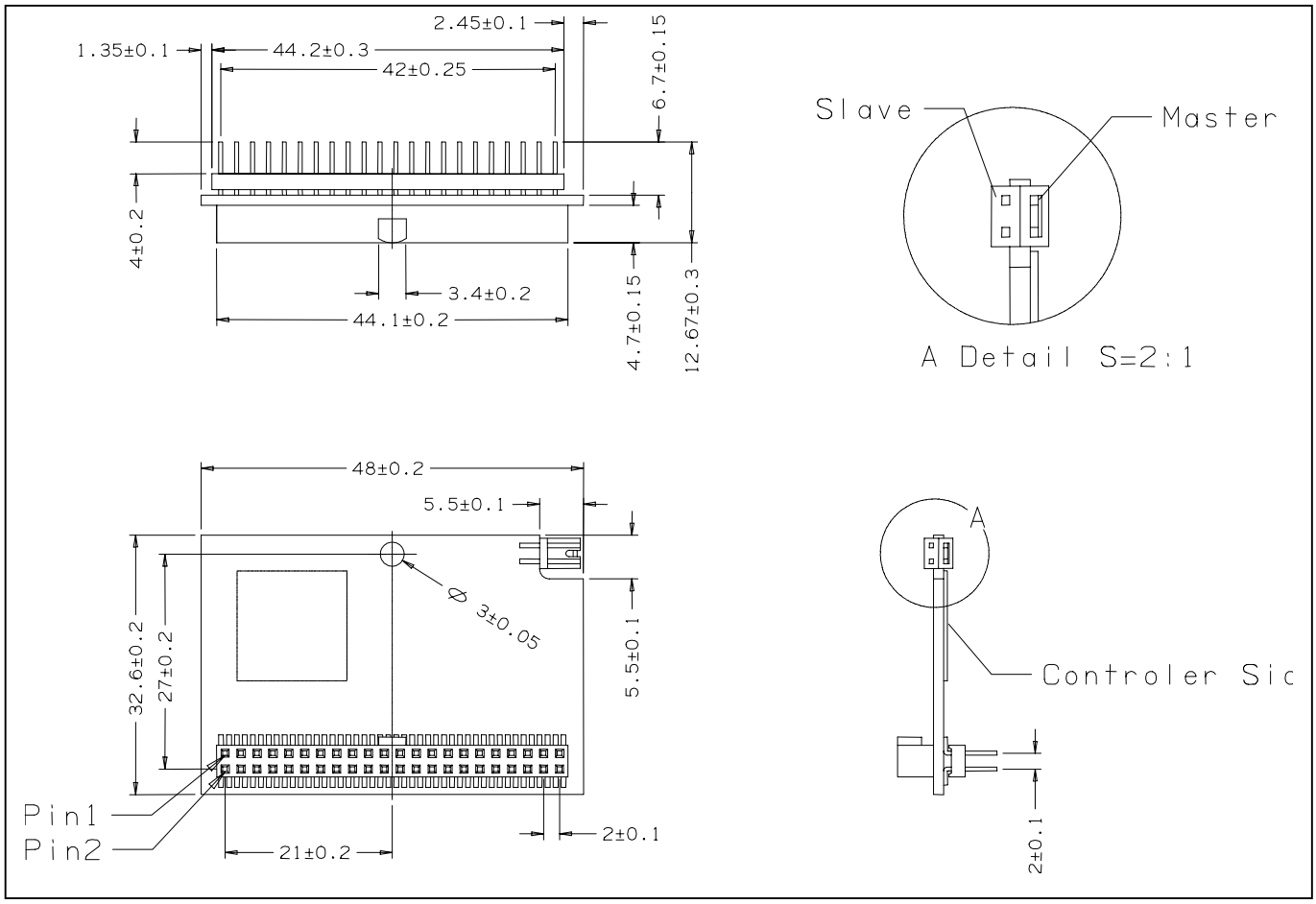
Physical Outline

FDXXX-426PA.XD4



Physical Outline

FDXXX-432LXX.XD4



Product Number	Controller Side Connector	Firmware Side Connector
FDXXX-432LMM.XD4	Male	Male
FDXXX-432LMF.XD4	Male	Female
FDXXX-432LMD.XD4	Male	×
FDXXX-432LFM.XD4	Female	Male
FDXXX-432LFF.XD4	Female	Female
FDXXX-432LFD.XD4	Female	×
FDXXX-432LDM.XD4	×	Male
FDXXX-432LDF.XD4	×	Female